APPLICATION OF STATISTICAL DESIGN AND RESPONSE SURFACE METHODS TO COMPUTER-AIDED VLSI DEVICE DESIGN

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Optimization of VLSI process/device design through computer simulation is a necessary step in the product cycle. Methodologies for determining an optimal operating point and analyzing its sensitivity to process and device perturbations are not well established. A statistical approach is ideally suited for this purpose. Adjustment of input factors through statistical design can desensitize the responses to variations in the inputs. This robustness is critical in designing for manufacturability. To demonstrate the applicability of this methodology, a BIMOS process was simulated using Suprem III and Sedan II. Based on the simulations, response surfaces were approximated, conflicting device requirements quantified, and a region of input factors satisfying the various response conditions was identified. While the proposed methodology is demonstrated for process/device simulation, it is equally applicable to the device/circuit stage.

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TO COMPUTER-AIDED VLSI DEVICE DESIGN

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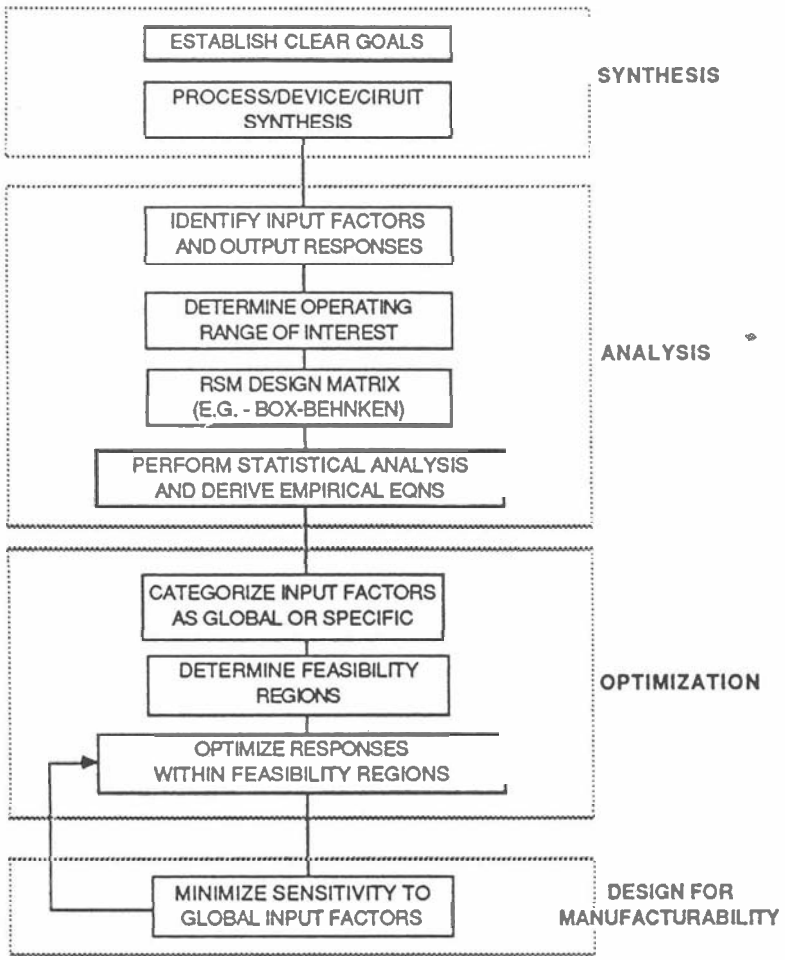
Optimization of VLSI process, device, and circuit design through computer simulation is a necessary step in the product cycle. Process, device, and circuit based strategies are available for **synthesizing** a nominal operating point based on engineering judgement. On the other hand, methodologies for simultaneously determining an optimal operating point and **analyzing** its sensitivity to process and device perturbations are less well established. If a sensitivity analysis is undertaken, the process or device designer typically resorts to "worst case" or ad hoc techniques, studies only a small number of potentially important factors and rarely takes into account interactions between these factors. Because of the complexity of VLSI product development an efficient strategy for studying the effect of a previous (nth) step in the design cycle on subsequent (nth+1) steps is required. A methodology based on **statistical** design and analysis techniques is ideally suited for this purpose. The approach can be briefly summarized:

1) Based on engineering knowledge identify input factors and response variables.
2) Determine the operating range of interest for the input factors and desired response levels.
3) Based on statistical guidelines choose an appropriate experimental design (matrix) over the space of input factors for performing simulations.
4) Perform the simulations.
5) Obtain response surfaces as functions of the significant input factors using regression analysis to approximate the simulated results.
6) Analyze results from **both** an engineering and statistical viewpoint.
7) Implement the results of the analysis.

A key step is (3), choosing the appropriate experimental points to be simulated. In this work, Box-Behnken response surface designs were used for this purpose. The Box-Behnken designs use a rather small number of data points to estimate the coefficients for all linear, quadratic, and first-order interaction terms in a polynomial model relating response variables to input factors. In this manner, a complete 2nd order model approximating the desired response in N-dimensional space is obtained. (N = number of input factors.) Design analysis is viewed as a multiple input-output system resulting in a **multiple constraints** optimization problem. Using the derived empirical equations for the response variables, mathematical optimization and sensitivity analysis can be performed within this constrained "desirability" space to determine optimal operating conditions. This leads to the concept of **global** input factors, which affect a large number of the response variables, and **specific** input factors which can be used to adjust the operating level of a small number of response variables. The proposed methodology can play a key role in **"designing for manufacturability"**. To demonstrate the applicability of this methodology to VLSI development every one-dimensional cross-section in an advanced BIMOS process was simulated using Suprem III and Sedan II. Based on the simulation results, response surfaces were approximated, conflicting device requirements quantified, and a region of input factors for which the various response conditions were simultaneously met was identified. It should be stressed that while the proposed methodology was demonstrated for one-dimensional process and device simulation, it is equally applicable to the device-circuit stage or to two-dimensional process-device simulation.



Flowchart For Statistical Approach to Simulation

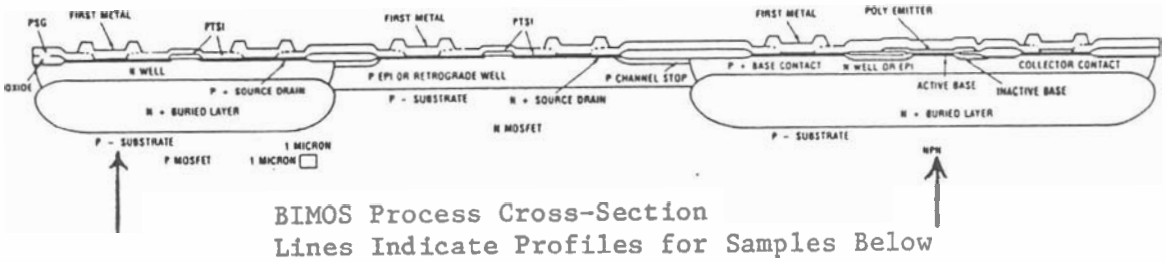
	X1	X2	X3	X4	X5	X6
FACTOR	TEPI	WELL DT	WELL DOSE	BASE DOSE	BASE KEV	GATE TOX
-		10'	1.5E+12	1	20	
0		30'	2E+12	1.5	35	
+		50'	2.5E+12	2	50	
	+	+	0	-	0	0
	+	-	0	+	0	0
	-	+	0	+	0	0
	-	-	0	-	0	0
	0	+	+	0	-	0
	0	+	-	0	+	0
	0	-	+	0	+	0
	0	-	-	0	-	0
	0	0	+	+	0	-
	0	0	+	-	0	+
	0	0	-	+	0	+
	0	0	-	-	0	-
	+	0	0	+	-	0
	+	0	0	-	+	0
	-	0	0	+	+	0
	-	0	0	-	-	0
	0	+	0	0	+	-
	0	+	0	0	-	+
	0	-	0	0	+	+
	0	-	0	0	-	-
	+	0	+	0	0	-
	+	0	-	0	0	+
	-	0	+	0	0	+
	-	0	-	0	0	-
	0	0	0	0	0	0

Input Factors

Levels

Design Matrix

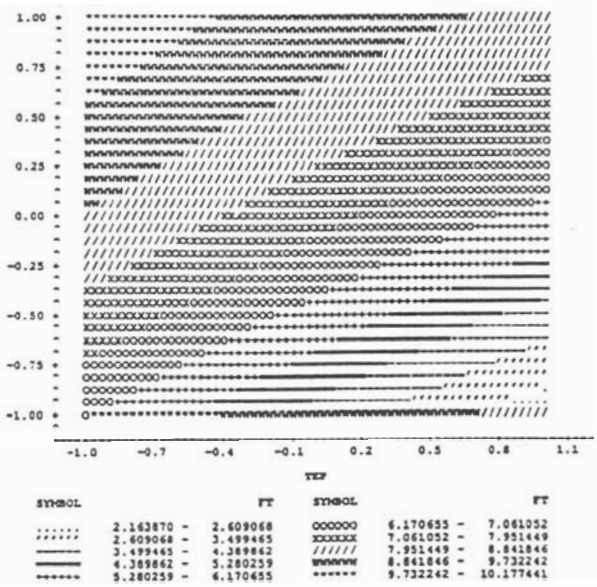
Box-Behnken Design Matrix



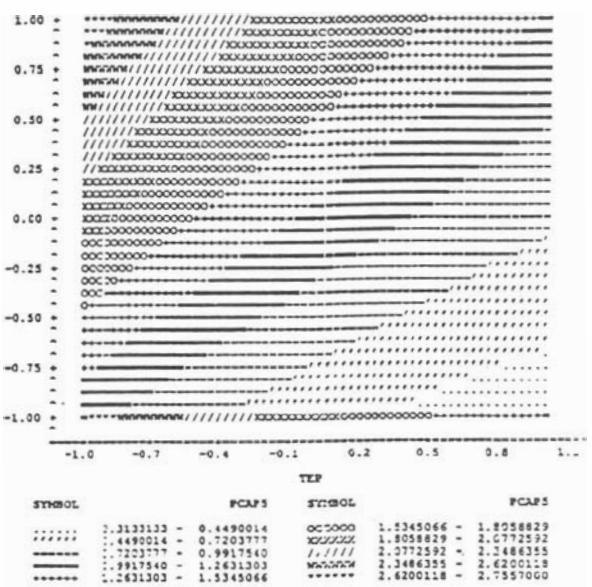
BIMOS Process Cross-Section
Lines Indicate Profiles for Samples Below

$$Ft = 4.6 - 0.78Tepi + 1.18WDt - 1.07BQ - 1.68BE - 0.59WDt^2 + 0.66Tepi*WDt + 0.65Tepi*BE - 0.48WDt*BQ - 0.93WDt*BE$$

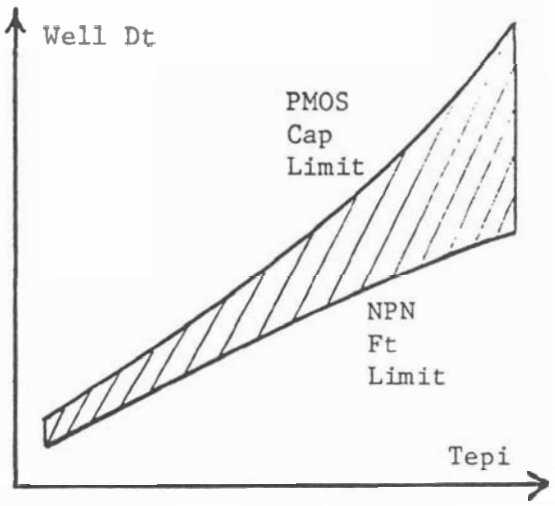
Example of Typical Empirical Eqn



Ft vs Tepi & Well Dt



PMOS Junction Cap vs Tepi & Well Dt



Superpositon of Desireability Regions For Ft & PMOS Junction Capacitance (Shaded Region)