# Performance Boost of GAA Si NS CFET via Tungsten Source/Drain Sidewalls

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## ABSTRACT

This study computationally analyzes the electrical performance of vertically stacked Gate-All-Around (GAA) Si nanosheet (NS) complementary FETs (CFETs) with (w/) and without (w/o) metal sidewall (MSW) structures in the source/drain (S/D) regions. MSW integration significantly reduces contact resistance and enhances drive current ($I_{on}$), though it slightly increases intrinsic capacitance. Without MSW, device and circuit performance are limited to a maximum of four channels due to weakened electrostatic potential from the top contact to the bottom S/D regions. In contrast, MSW structures, leveraging tungsten's low resistivity ($5.6 \times 10^{-6}$ Ω·cm), support higher $I_{on}$ and improved scalability, enabling performance gains beyond four channels. For instance, a 10-channel CFET with MSW achieves a 56.9% higher ring oscillator (RO) frequency compared to w/o MSW devices. These results highlight the critical role of MSW in optimizing advanced designs of emerging GAA Si NS CFETs.

## INTRODUCTION

Due to the severe short-channel effects (SCEs) and weakened gate controllability, scaling of devices has caused a sizeable leakage current. To overcome this bottleneck, GAA devices, such as NS, have been of special interest because they can reduce supply voltages, sustain gate drivability, and achieve high performance for advanced technology nodes. The stacking of N- and P-FETs vertically is one of the primary benefits of using CFETs, which allows for a considerable reduction in active area [1]-[7]. However, to minimize the DC performance loss by NS resistance, there were many efforts to reduce the contact resistivity at the semiconductor/silicide interface.

In this study, we numerically investigate the impact of MSW integration on electrical characteristics of both N/P-FETs in CFET and three-stage CFET ring oscillators.

## 3-D COMPUTATIONAL DEVICES

Fig. 1(a) presents a 3-D schematic, and Fig. 1(b) is a 2-D schematic of the GAA Si NS CFET, consisting of a bottom P-FET and a top N-FET [8], [9]. The device simulation employs the quantum-mechanically corrected transport models, along with four mobility models: the high-field saturation, the Philips unified model, the Lombardi model, and the ballistic mobility. In addition, Hurkx band-to-band tunneling and Shockley-Read-Hall recombination are included to account for generation and recombination effects.

## RESULTS AND DISCUSSION

Figure 2 shows the SCEs in CFETs w/ and w/o MSW, considering varying number of channels in N- and P-FETs. Fig. 2(a) highlights the off-state current ($I_{off}$) trends, revealing a 35.8% reduction for N-FETs and a 22.4% reduction for P-FETs in devices w/ MSW compared to those w/o MSW. This reduction in $I_{off}$ with increasing number of channels in w/ MSW devices is primarily attributed to enhanced electrostatic control, reduced parasitic resistance, and improved charge confinement, which collectively suppress SCEs and minimize leakage currents. Enhanced gate-to-channel coupling in GAA structures w/ MSW ensures more effective control over the channel potential, mitigating drain induced barrier lowing (DIBL) and subthreshold leakage. Fig. 2(b) demonstrates a 68.7% increase in $I_{on}$ for 10-channel N-FETs w/ MSW compared to w/o MSW devices. This improvement stems from the reduced series resistance at the S/D contacts due to the integration of low-resistivity tungsten in the sidewalls, which enhances carrier injection efficiency and minimizes voltage drop at the S/D junctions. Additionally, improved electrostatic control ensures a more uniform potential profile across vertically stacked channels, optimizing carrier transport and drive strength. Furthermore, Fig. 2(c) analyzes DIBL, demonstrating that variations number of channels have minimal impact on DIBL in both w/ MSW and w/o MSW devices, indicating stable threshold voltage ($V_{th}$) control across multiple channels. Fig. 3(a) further confirms that the $V_{th}$ remains constant as the number of channels increases, a characteristic attributed to the strong electrostatic confinement provided by the GAA architecture.

Gate capacitance ($C_G$) is a critical AC parameter, directly extracted from the AC response curves of N- and P-FETs. As shown in Fig. 3(b), $C_G$ increases with the number of channels due to the larger cumulative channel surface area, allowing greater charge accumulation and facilitating linear capacitance scaling. This increase is further supported by parallel capacitance addition and improved electrostatic coupling between the gate and channel, which collectively enhance carrier confinement and mitigate SCEs. Fig. 4 presents a 2-D current density profile at the middle of the channel in the on-state for N- and P-FETs w/ and w/o MSW. The significantly higher current density in w/ MSW devices is attributed to enhanced electrostatic control and reduced series resistance (Fig. 5), resulting in improved carrier velocity and overall current conduction efficiency. Fig. 6 compares the RO frequency vs. number of channels. Beyond four channels, the frequency decreases for devices w/o MSW due to increased parasitic resistance and capacitance, which degrade signal propagation speed. In contrast, w/ MSW devices exhibit a 56.9% increase in frequency, driven by improved electrostatic control, lower resistance. The performance boost highlights the effectiveness of MSW in mitigating channel-induced degradation, making it essential for high-speed applications.

## CONCLUSION

In summary, GAA Si NS CFETs w/ MSW outperform w/o MSW configurations due to reduced S/D resistance from the low-resistivity tungsten sidewalls. While both $I_{on}$ and parasitic capacitance increase number of channels, $I_{on}$ growth slows and saturates for w/o MSW devices when the number of channels exceeds four, due to diminished electrostatic potential from top to bottom channels.

## ACKNOWLEDGMENT

This work was supported in part by the National Science and Technology Council (NSTC), Taiwan, under Grant NSTC 113-2221-E-A49-094 and Grant NSTC 113-2218-E-006–019-MBK, and in part by the 2025 JDP of TSMC.

## REFERENCES

[1] S. R. Kola *et al.*, *IEEE T. Nano*, vol. 23, pp. 382–392, 2024.
[2] X. Yang *et al.*, *IEEE T. ED*, vol. 70, pp. 3935–3942, 2024.
[3] X. R. Yu *et al.*, *IEDM*, pp. 487–490, 2022.
[4] B. Vincent *et al.*, *IEEE J. EDS*, vol. 8, pp. 668–673, 2020.
[5] Y. Li *et al.*, *IEDM*, pp. 887–890, 2015.
[6] X. Yang *et al.*, *IEEE T. ED*, vol. 69, pp. 4029–4036, 2022.
[7] C. Y. Huang *et al.*, *IEDM*, pp. 20.6.1-20.6.4, 2020.
[8] S. R. Kola *et al.*, *ISQED*, pp. 1-6, 2023.

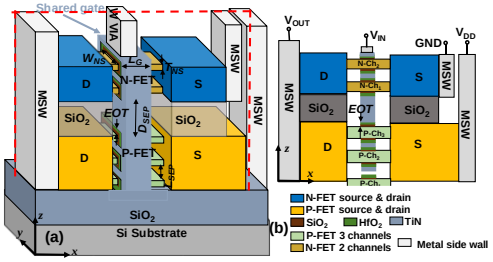


Fig. **1**. (a) 3-D schematic of the GAA Si NS CFET w/ MSW. (b) 2-D cross-sectional view (cut-$C_1$) of the device. The channel count is further increased to ten.

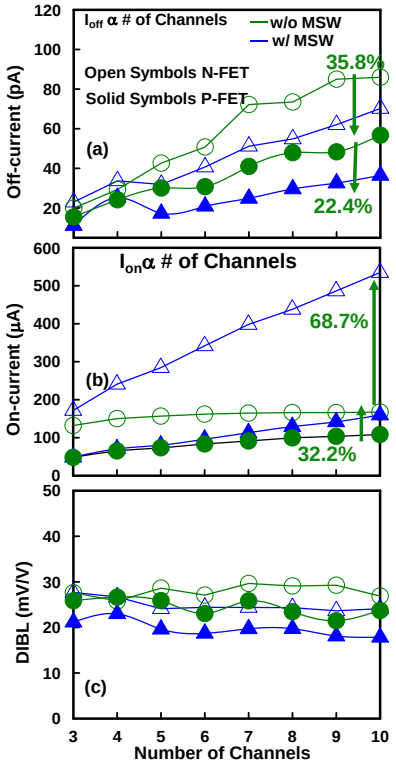


Fig. **2**. The impact of number of channels on SCE parameters in GAA Si NS CFETs. (a) $I_{off}$ and (b) $I_{on}$ vs. the number of channels. For devices w/ MSW, the $I_{on}$ is enhanced by 68.7% for N-FETs and 32.2% for P-FETs compared to devices w/o MSW. This improvement highlights the effectiveness of MSW in boosting carrier transport and overall device performance. (c) DIBL vs. the number of channels.

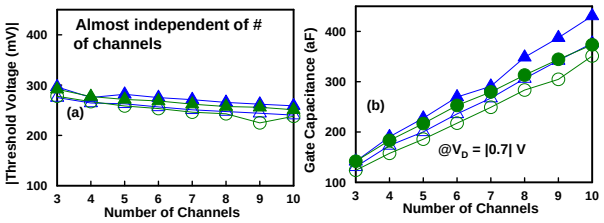


Fig. **3**. (a) The $V_{th}$ versus the number of channels for both N- and P-FETs in CFET devices, demonstrating that $V_{th}$ remains largely unaffected by number of channels, indicating stable electrostatic control. (b) $C_G$ increases with number of channels due to expanded channel surface area, allowing for greater charge accumulation and enhanced electrostatic coupling between the gate and channel.

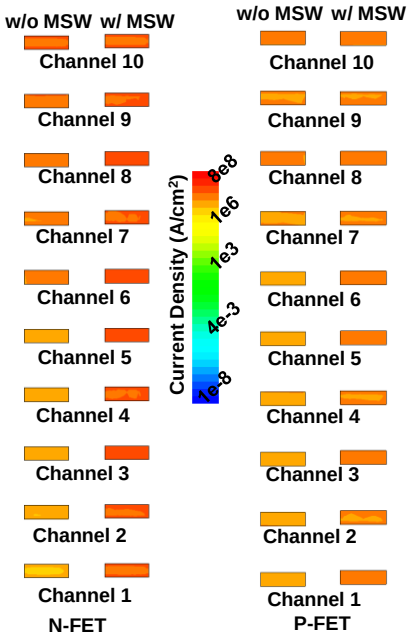


Fig. **4**. The 2-D current density distribution profile at the middle of the channel in the on-state condition ($|V_G| = |V_D| = 0.7$ V), illustrating carrier transport characteristics and highlighting the impact of electrostatic control on current flow in the device.

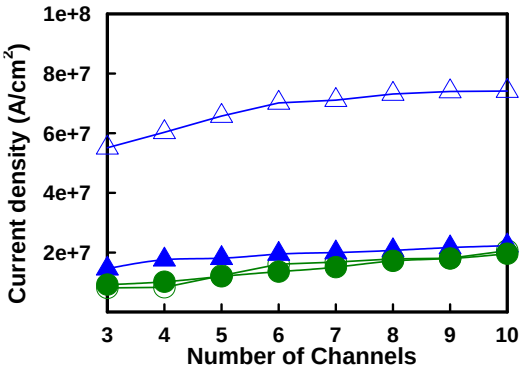


Fig. **5**. The current density vs. the number of channels at the middle of the channel under on-state conditions. Devices w/ MSW exhibit a significant increase in current density, attributed to reduced S/D resistance and enhanced electrostatic control.

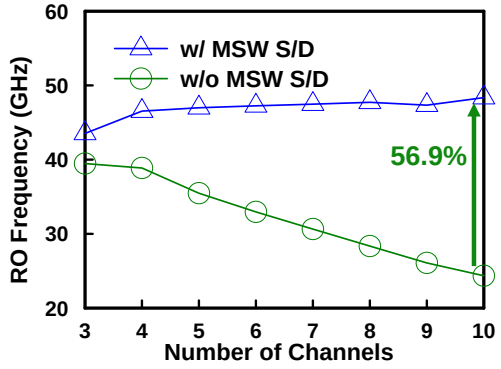


Fig. **6**. The RO frequency vs. the number of channels for the devices w/ and w/o MSW. In the w/o MSW, frequency declines as number of channels increases, primarily due to higher resistance in the top S/D regions.