Self-Heating and Hot Carrier Degradation Interaction in 28-nm FD-SOI pFETs

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Self-heating effect (SHE) and hot carrier degradation (HCD) are two significant and well-known reliability issues in CMOS technology. Both these effects degrade device parameters such as drain current and transconductance, the former being the performance degradation due to temperature effects, while the latter is due to the build-up of defects in the device structure. SHE becomes critical in structures with poor thermal conductivity — such as SOI and thin-film transistors—, while HCD depends directly on the electric field along the channel. Nevertheless, these effects are far from independent mechanisms. Even though their interplay is minimal for *n*-channel devices, it is known that SHE accelerates HCD in *p*-channel FETs [1]. To investigate the underlying relationship between SHE and HCD, electrothermal Monte Carlo simulations were carried out for a 28-nm technology FD-SOI pFET. The device structure of interest, depicted in Fig. 1, has a physical channel length of 30 nm, width of 80 nm, silicon film thickness of 7 nm, gate oxide thickness of 1.2 nm, and a 25-nm layer of BOX over a 50-nm thick *p*-type silicon substrate. Simulated $I_{DS} \times V_{GS}$ characteristic for one MC seed is shown in Fig. 2 and compared to available experimental data [2]. The results present good agreement for the entire bias range, yet mainly for the strong inversion region, which is the most relevant in the context of this work. Non-isothermal simulations were carried out using the framework presented in [3] considering a bias point of $V_{GS} = V_{DS} = -0.9$ V and 300 K fixed-temperature thermal boundaries at the back, source, and drain contacts. Both temperature and thickness of the silicon film were accounted for when considering the thermal conductivity degradation, which reaches no more than 7 $\mathrm{W/mK}$ for the temperature range of the device, in contrast to the 130 $\mathrm{W/mK}$ bulk value used in the substrate. The lattice (acoustic phonon) temperature T_L, depicted in Fig. 3, reaches up to 328 K at the drain side of the channel. At the same point, optical phonon temperature T_{OP} may exceed 380 K under the same circumstances, evidencing the non-equilibrium between the phonon baths. Increased T_L and T_{OP} enhances all types of scattering mechanisms, i.e., acoustic phonon (ACOU) and non-polar optical phonon emission (E) and absorption (A) for holes residing in all three valence bands (heavy hole (HH), light hole (LH) and split-off (SO)), as depicted in Fig. 4. In our framework, increased T_{OP} enables more carriers to interact with the optical phonon bath and eventually absorb energy. Fig. 5 depicts the hole energy distribution for the entire device. Even though the energy tends to decrease slightly on average for non-isothermal simulation due to enhanced phonon emission scattering, the increase in phonon absorption events results in even higher energies for some carriers, extending the tail of the distribution. These carriers will likely contribute to HCD since their energy surpasses the impact ionization threshold of 1.8 eV. Moreover, they can also increase their contribution to BTI by occupying charge traps whose energy level was once unreachable. Fig. 6 depicts how the energy distribution evolves as a function of the position along the device length ($L_{tot} = 48$ nm). At the source ($L_{tot}/6$), where T_L and T_{OP} are smaller, there is almost no difference between isothermal and non-isothermal results. However, as the position moves towards the hot spot ($2L_{tot}/3$) and beyond ($5L_{tot}/6$), the increase in the distribution tail due to SHE becomes evident.

REFERENCES

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[2] M. Casse et al., IEDM (2022). DOI: 10.1109/IEDM45625.2022.10019322.

[3] A.C.J. Rossetto et al., J. Comput. Electron. **20**, 1644 (2021). DOI: 10.1007/s10825-021-01740-5.

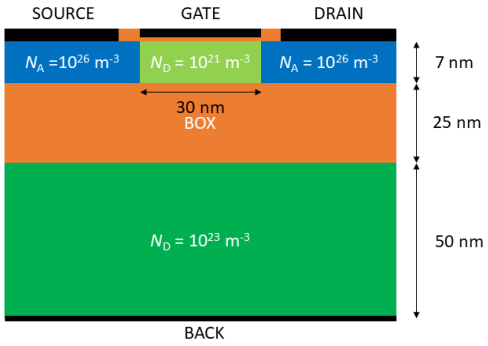

Fig. 1. PMOS FD-SOI case-study structure.

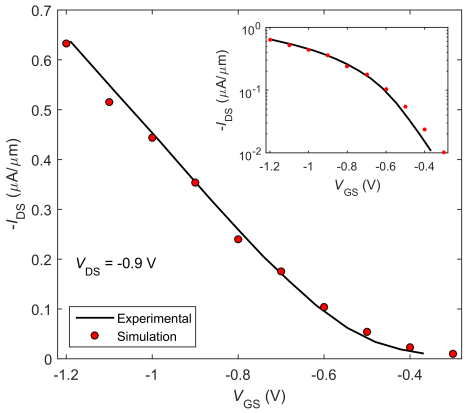

Fig. 2. $I_{DS} \times V_{GS}$ characteristics for the case-study device.

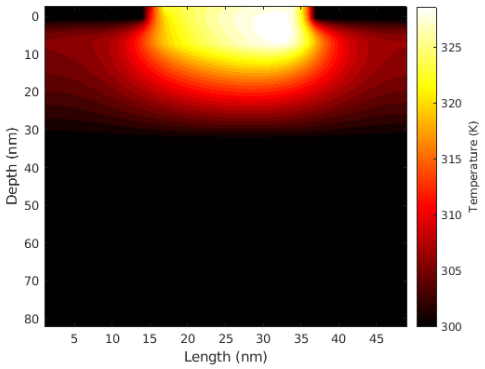

Fig. 3. Lattice temperature profile averaged along the device width.

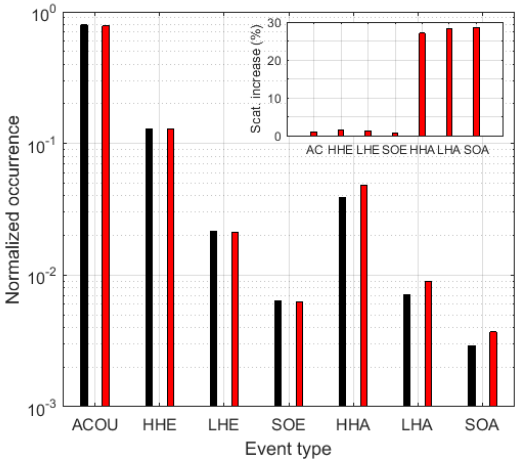

Fig. 4. Normalized occurrence of scattering events for each mechanism in isothermal and non-isothermal simulation.

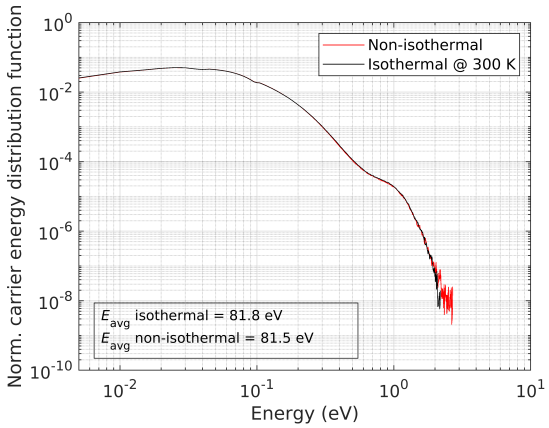

Fig. 5. Normalized hole energy distribution function for isothermal (black) and non-isothermal (red) simulation considering the entire device.

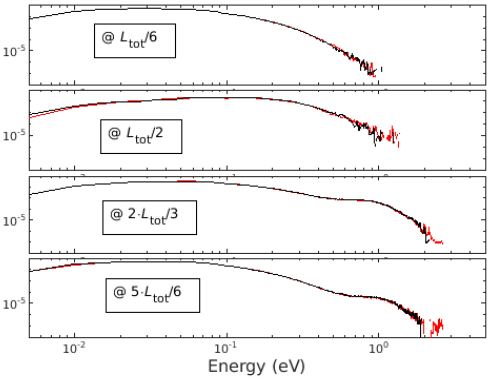

Fig. 6. Normalized hole energy distribution function for isothermal (black) and non-isothermal (red) simulation at different positions along the device length.