Temperature-Dependent Electric Switching of Chalcogenide Memories Below the ns Limit

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Abstract — A space- and time-dependent transport model in amorphous chalcogenides, including both localised and mobile electron states, is used here to explore the kinetics of threshold switching of nanoscale structures in the ns–ps time domain. The analysis is carried out in the high-temperature range (below the phase-transition temperature), to test the effect of lattice temperature on the ultrafast switching in view of a possible exploitation in automotive applications.

State of the art and model — Chalcogenide-based Phase Change Memories (PCM) have been studied for many years as a possible replacement for Flash memories [1, Ch. 30 and Refs. therein]. Being two-terminal devices with fast access time and moderate cost, they were easily integrated in 3D cross-point memory arrays [2], with potential breakthroughs in industrial applications; among these, automotive applications [3]. PCM action relies on the fast and reversible structural change of a chalcogenide alloy that switches between the amorphous (*reset*) and crystalline (*set*) states upon the application of an electric pulse [4]. A voltage pulse of suitable intensity, and width of a few ns is often required to surpass an off-to-on threshold switching in the amorphous state (Ovonic Threshold Switching—OTS), precursor of the amorphous-to-crystalline phase change. The limits of a fast electric switching for both selectors and memory elements, based on chalcogenides, are related to the above-mentioned OTS, and to the crystallization kinetics after it [5], [6]. Achieving sub-ns threshold-switching times for nanoscale devices is a goal of both scientific and technological relevance [7], [8]. Preliminary analyses [9] were implemented to interpret recent experimental results in the ns–ps time domain. Here the approach is extended to a range of temperatures of interest for automotive applications, and tested for applied external voltages produced by optimised electric configurations. Following [10], a homogeneous chalcogenide is considered, in one dimension, assuming unipolar conduction with localised and mobile states. Numerical solutions of the model equations for a time-dependent bias were carried out, varying the thermal-bath temperature from room to high temperatures (always below the amorphous-crystalline transition one). Voltage pulses with finite rise and fall times as fast as 1.5 ns (comparable with the microscopic relaxation times) were considered, as in the experiments of [8].

Results — The transport model has been applied to a 53-nm thick GST-225 chalcogenide layer [9]. Pulses with different plateau values and duration were used, along with different lattice temperatures T, above room temperature and below the crystallization one (425 K); the goal was testing how the transient of the electric current and, in particular, the OTS are affected by an extended temperature range. It was found that the threshold voltage V_{th} decreases at increasing temperatures (specifically, $V_{\mathrm{th}} = 2, 1.4, 1.1$ V at $T = 298, 350, 400$ K, resp.); this is due to an increase in the mobile-carrier concentration, whence in the current triggering the onset of OTS. Fig. 1 shows the applied voltage and the current through the device as functions of time, at $T = 350$ K, for one of the simulated voltage profiles. Fig. 2 shows the currents obtained at different temperatures for a given voltage profile. Fig. 3 shows the time evolution of the electron temperature T_e for the same voltage profile as in Fig. 2 (as shown in [12], T_e is almost constant in space). Finally, Fig. 4 shows the delay time as a function of T for two different plateau voltages. To conclude, ultrafast transient characteristics (in the ns scale and below) have been obtained for all temperatures considered. This indicates that ultrafast, sub-ns electric switching of chalcogenide memories can be exploited in automotive applications.
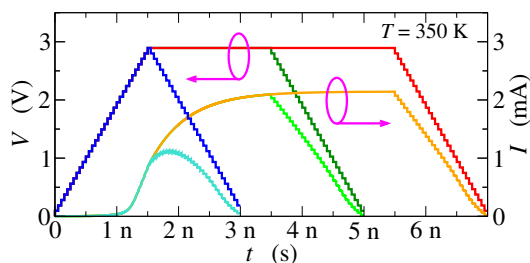
Fig. 1. Current flowing across the PCM device as a function of time (right scale) after the application of voltage trapezoidal profiles of 2.8 V amplitude (left scale), at $T = 350$ K. Rise and fall times are 1.5 ns in all cases, whereas the plateau durations are 0, 2, and 4 ns. The duration of the plateau influences the maximum value of the current, but does not affect the rise time
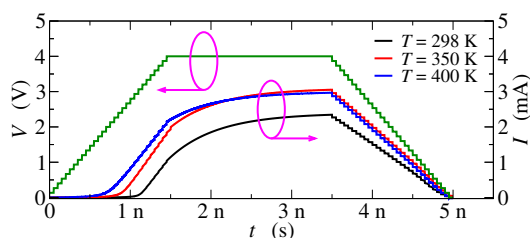

Fig. 2. Currents (right scale) corresponding to a 4-V amplitude and 2-ns plateau duration, at different temperatures. At higher lattice temperatures not only a larger current is obtained, but also the increase in the current occurs earlier: this is due to an increased efficiency of the carrier-heating process at the origin of the OTS effect.
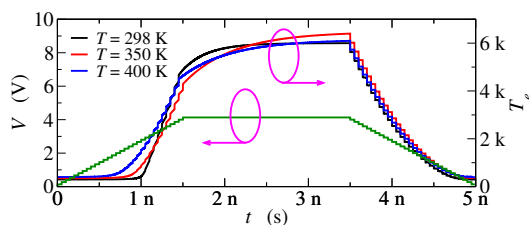

Fig. 3. Time evolution of the electron temperature T_e (right scale) for a 4-V amplitude and 2-ns duration of the voltage plateau. The interpretation derived from Fig. 2 is confirmed by the trend of the electron temperature shown here, where the heating process sets in at shorter times for temperatures above room temperature. As a consequence of the above picture, the
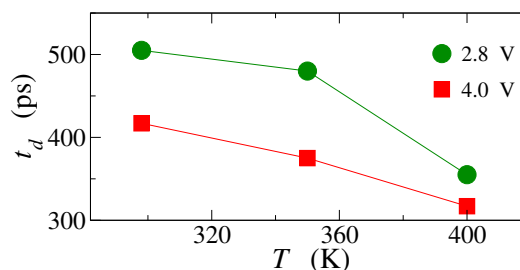

Fig. 4. Simulated delay time t_d as a function of the lattice temperature T for two plateau voltages (2.8 and 4 V); t_d is the time interval between the instant at which the applied voltage exceeds the threshold value and the instant at which a steep rise in the device current begins [7], [11], and is a useful parameter for quantifying the switching speed of the electric response.

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