Compact modeling of memristors for neuromorphic circuit simulation

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INTRODUCTION

The combination of memristors and CMOS circuits is a promising strategy for the hardware implementation of neural networks (NN) for IoT applications. A compact device model is a simple math. description of its electrical characteristics, to accurately represent its behavior in a circuit. In this work, we present a compact model for filamentary resistive switching (RS) devices with the final goal of simulating memristive circuits. Our model is based on Chua's memristor theory and it includes two coupled equations, one for the current and one for the internal memory parameter (see Fig.1) [1].

MODEL

The memory equation implements the competition of SET and RESET processes with voltage-dependent characteristic times. The current equation is based on the theory of conduction through point contacts. Results of the model for I(V) loops and the conductance hysteron are shown in Fig. 2. Although initially thought for filamentary devices, the model also works for homogeneous RS. Finally, the model has been generalized for memristors showing conductance quantization.

PARAMETER EXTRACTION

The model has ten parameters and we have used a convolutional NN dealing with images of the I(V) loops. The method provides similar results to those of the least-square method (LSM) (Fig. 3) but requires one order of magnitude less time for large number of cycles (10^4–10^5), enabling to deal with switching statistics. With the extracted parameters, the model matches the experimental characteristics as shown in Fig. 4.

SIMULATION OF NEURAL NETWORKS

As an example of application to neuromorphic circuits, we have simulated a simple NN for the recognition of hand-written digits (MNIST database). For the implementation in SPICE, we have converted the memory equation into a very simple equivalent circuit based on a capacitor and two current sources. The NN is a single-layer perceptron with two memristor crossbar arrays for positive and negative weights. Approximately, the simulated circuit contains 16k memristors and about 20k MOSFETs for the control electronics. Training is performed in software and both the writing of weights and the performance during the inference phase have been considered [2]. As an example, Fig. 5 shows the simulated accuracy loss of the network due to wire parasitic resistance (R_W). This is done both as a function of the array size (image resolution) and the ON resistance (R_{ON}). The model performance in terms of memory use and computation time is comparable to much simple models while it provides a much better description of the device behavior (see Fig. 6).

CONCLUSION

A simple compact model for memristors and a novel method for extracting its parameters have been presented. Successful simulation of a memristor based NN has been shown. Extension of the model to devices showing different discrete quantum conductance levels has also been developed and simulation of NN performed.

ACKNOWLEDGMENT

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[1] E. Miranda and J. Suñé, IEEE Trans. Nanotechnol. 2020, 19, 837–840.[2] F. Aguirre et al., Frontiers in Phys.9, 735021 (2021)

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda, V_C)} - \frac{\lambda}{\tau_R(\lambda, V_C)}$$

$$\lambda \downarrow$$

$$I = G_0 N V + \frac{2e}{h\alpha} ln\left(\frac{1+e^{\alpha(\Phi-\beta eV)}}{1+e^{\alpha[\Phi+(1-\beta)eV]}}\right)$$

Fig. **1**. The two equations defining the compact model. The internal memory parameter, λ, is related to ion movement, and it couples both equations. The I(V) equation is related to conduction through a parabolic potential barrier associated to a quantum constriction. Φ is the barrier height, α is related to the barrier width, β describes the possible asymmetry of voltage drops at the interfaces, and N is the number of conducting modes.

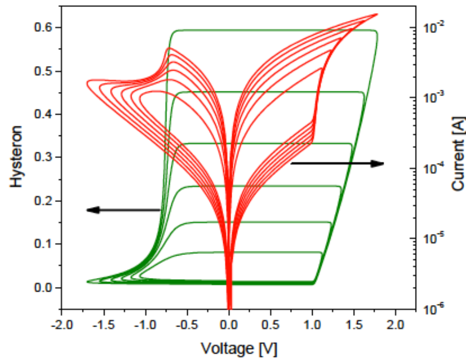

Fig. 2 Switching loops and conductance hysterons (including intermediate states) simulated by the model.

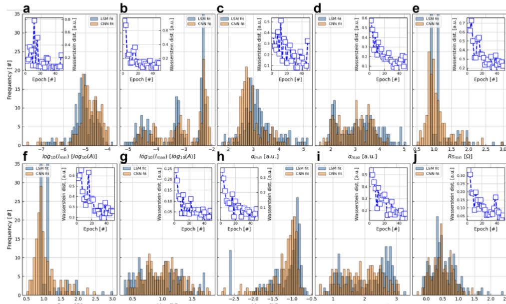

Fig. 3. Statistical distribution of parameters for successive loops in a single device compared to LSM extraction method.

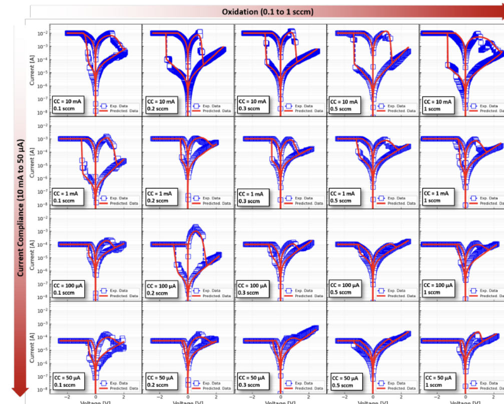

Fig. 4. Simulated I(V) loops with the extracted parameters

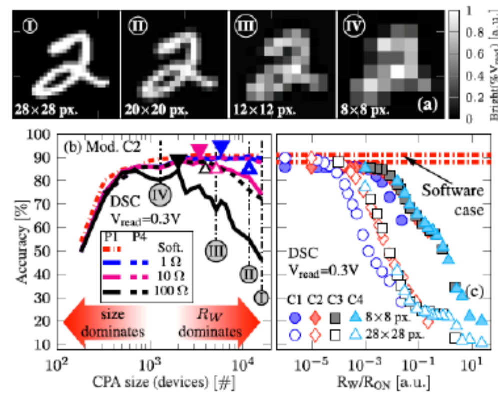

Fig. 5. Effects of the wire resistance on network accuracy as a function of crossbar array size and ON device resistance.

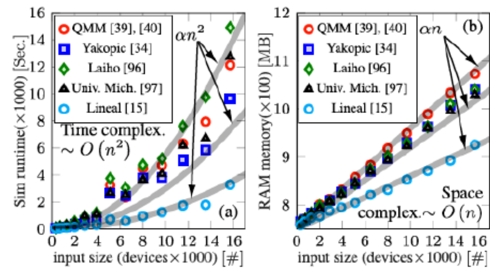

Fig. 6. Performance of different compact models for the simulation of the neural network in terms of memory use and computing time.