# Electrothermal Properties of 2D Materials

S. Klein[1], Z. Aksamija[2]
[1]University of Massachusetts, Amherst, MA, USA, [2]University of Utah, Salt Lake City, UT, USA,
email: zlatan.aksamija@utah.edu

***Abstract*—**To keep downsizing transistors, new materials must be explored. 2D materials are appealing due to their thinness and bandgap. The relatively weak van der Waals forces between layers in 2D materials allow easy exfoliation and device fabrication but also result in poor heat transfer to the substrate, which is the main path for heat removal. The impaired thermal coupling is exacerbated in few-layer devices where heat dissipated in the layers further from the substrate encounters additional interlayer thermal resistance before reaching the substrate, which results in self-heating ($\boldsymbol{\Delta T \neq 0}$ where $\boldsymbol{\Delta T}$ is the temperature rise of the few-layer device) and degradation of mobility. This study explores the electrothermal properties of five materials ($MoS_2$, $MoSe_2$, $WS_2$, $WSe_2$, and 2D black phosphorous). We simulate various devices with self-heating with various $V_{DS}$ and examine the effects on mobility and change in device temperature and compare to the isothermal case ($\boldsymbol{\Delta T = 0}$). We observe that self-heating has a significant effect on temperature rise, layer-wise drain current, and effective mobility. We show that black phosphorous performs the best thermally and $WSe_2$ performs the best electrically. This study will inform future thermally aware designs of nano electronic devices based on 2D materials.

## I. Introduction

As transistors continue to become smaller, traditional 3D materials such as silicon become problematic as quantum effects prevail [1]. New materials must be explored to continue downsizing semiconductors. 2D materials such as transition metal dichalcogenides (TMDs) and 2D black phosphorus (phosphorene) are attractive replacements as they are thin and contain a bandgap [2]. Mobility suffers in single-layer devices [3] due to charged impurity scattering from the substrate. To resolve this issue, few-layer stacks are explored, using the layers immediately above the first layer to encapsulate the bottom [4]. This results in improved mobility but creates more thermal issues. Heat removal is more difficult in upper layers as they are farthest from the substrate, which dissipates the most heat from the device [5], and the layers create additional interlayer thermal resistance [6] due to weak van der Waals forces between 2D layers [7]. This results in self-heating and a degradation of mobility.

In this study, the four TMDs ($MoS_2$, $MoSe_2$, $WS_2$, and $WSe_2$) as well as 2D black phosphorus (BP) are compared. We look at several electrical properties (drain current and mobility) and multiple thermal properties (temperature rise, joule heating, mobility degradation, TBC, and effective conductivity) to determine what material has the best balance between electrical and thermal performances.

## II. Methods

The device being simulated is a back-gated MOSFET, composed of 10 layers. The source and drain contacts are connected to the topmost layer with the substrate and gate below the bottommost layer. Each layer has a different resistance, voltage, and current flowing through it. The current encounters extra resistance via interlayer resistance as well as the contact resistance above the topmost layer. The device can be represented as a resistor network, composed of layer resistance, interlayer resistance, and contact resistance, which is used to calculate layer-wise voltage and current. We use the coupled Schrodinger-Poisson equations to calculate carrier concentration per layer ($Q_i$) and screening length per layer ($\lambda_i$), from which mobility per layer is calculated using $\mu_i = \mu_1 + (\mu_\infty - \mu_1)(1\text{-}c_i)$ where $c_i = c_{i-1}\,(\exp(-d_{ML}/\lambda_i))$ and $d_{ML}$ is the thickness of the layer. We calculate layer-wise resistivity using $\rho_i = m/Q_i e\mu_i \cdot L_{channel}$ where $m$ is the fraction of the channel not pinched off, $e$ is the magnitude of the charge of an electron, and $L_{channel}$ is the length of the channel. We then calculate the total resistivity in the device by adding the interlayer resistances ($R_{int}$) and contact resistances in series with the layer resistivity and then add those values in parallel. Temperature rise per layer is calculated from

$$\Delta T_i = \left(\frac{P_i}{W_{ch}L_{ch}}\right) R_{BD,i}\left[1 - \frac{2L_{H,i}}{L_{ch}}\tanh\left(\frac{L_{ch}}{2L_{H,i}}\right)\right],$$

where $L_{H,i} = \sqrt{\kappa_{bulk} d_{ML} R_{BD,i}}$. $R_{BD,i}$ is the layer-wise thermal boundary resistance ($R_{BD,i} = 1/h_{BD,i}$), $\kappa_{bulk}$ is the bulk thermal conductivity, and $W_{channel}$ is the channel width. The simulation is iterated until convergence is reached (Fig. 1).

## III. Results

We first look at the $I_D$-$V_{DS}$ characteristics of the five materials for both the isothermal case and the self-heating case where $I_D = \sum I_i$ in Fig. 2. $WS_2$ has the most current and BP has the least in the isothermal case. However, current degradation due to self-heating is greatest for $WS_2$ and $MoS_2$, so $WSe_2$ has the most current in that case and $MoS_2$ has the least. Total joule heating ($P = \sum P_i$) (in Fig. 3) follows the same trend as the $I_D$-$V_{DS}$ characteristics. $WS_2$ experiences the most joule heating in the isothermal case, but $WSe_2$ experiences the most with self-heating. BP has the least isothermally and $MoS_2$ has the least with self-heating. Next, we look at average temperature rise ($\boldsymbol{\Delta T_{avg}}$) vs $V_{DS}$ in Fig. 4. $WS_2$ and $WSe_2$ undergo the most self-heating and BP self-heats the least. We calculate effective thermal conductance using $G_{eff} = P/\boldsymbol{\Delta T_{avg}}$ in Fig. 5. BP is shown to have the highest $G_{eff}$ which makes sense given that BP has the lowest amount of self-heating. $MoS_2$ has the lowest conductance.

Next, we look at the ratio of carrier mobility in the self-heating case to the isothermal case per layer in Fig. 6. Overall, $WS_2$ experiences the largest amount of mobility degradation. BP and $WSe_2$ experience the least. Factoring in phonon-limited mobility, with self-heating, $WS_2$ and $WSe_2$ have the highest upper layer mobility and $MoSe_2$ and BP have the lowest. Thermal boundary resistance (TBR), calculated by taking the inverse of TBC, is plotted for each layer. $MoS_2$ has the highest TBR and BP has the lowest.

## IV. References


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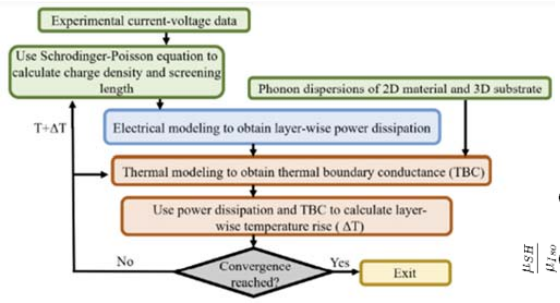



Fig. 1. Flowchart of our self-heating loop showing electronic and thermal components of the simulator.

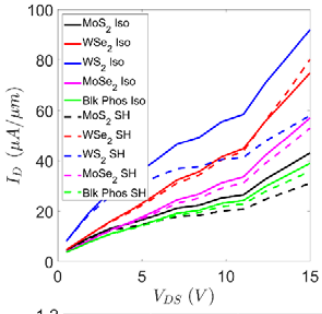



Fig. 2. IV-curve at $V_g$ = 6V for both the isothermal (dashed) and self-heating case (solid lines).

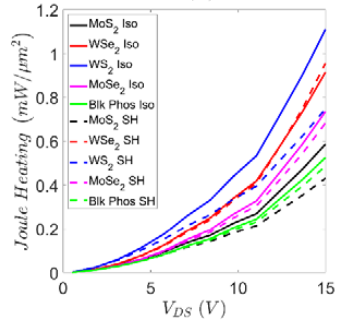



Fig. 3. Joule heating for various $V_{DS}$ at $V_g$ = 6V for both the isothermal (dashed) and self-heating case (solid lines).

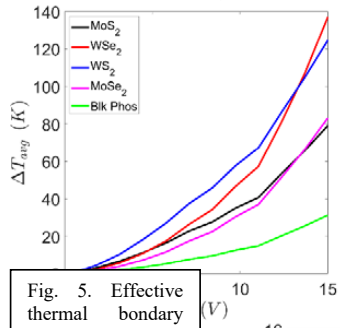
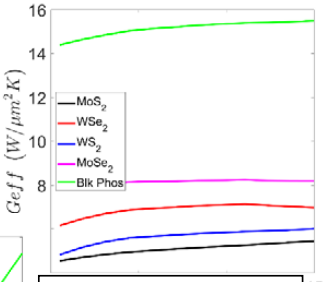



Fig. 4. Average temperature rise as a function of $V_{DS}$ at $V_g$ = 6V for all 5 materials under consideration showing lowest rise in BP and highest in $WSe_2$.

Fig. 5. Effective thermal bondary conductance into the substrate as a function of $V_{DS}$ at $V_g$ = 6V. BP shows the highest conductance.



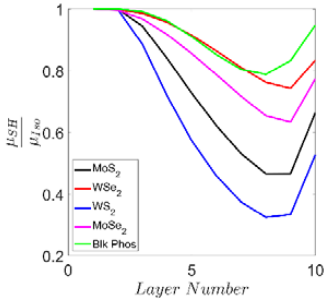




Fig. 6. Ratio of layer-wise mobility in the self-heating case to layer-wise mobility in the isothermal case at $V_{DS}$=15V and $V_g$=6V