3D Multi-Level-Set Simulation of Bottom Dielectric Isolation Process for Forksheet FETs

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ABSTRACT

The effect of a Si separator layer in the bottom dielectric isolation (BDI) process for forksheet field effect transistors (FSFETs) has been numerically investigated by an in-house topology simulator based on the 3D multi-level-set method. From the simulation result, it is clearly seen that the geometric profile of $Si_{0.8}Ge_{0.2}$ sacrificial layer can be improved by adding the Si separator layer.

INTRODUCTION

The FSFET has emerged as a next generation device architecture with its N/P space scaling potential [1], [2]. The reduced N/P space in the FSFET can cause difficulty in an opposite polarity doping for the junction-based substrate isolation, and the challenging process can be eliminated by introducing the BDI [2]. However, the $Si_{0.8}Ge_{0.2}$ sacrificial layer may be damaged in the BDI process, causing problems in the gate contact formation process. Therefore, it is essential to examine the geometric profile of the device after the BDI process. The multi-level-set method can accurately represent and evaluate the boundary evolution of the multiple materials [3]. Hence, it is suitable to investigate the geometric profile of the FSFET after the BDI process.

In this work, we numerically simulate the BDI process of the FSFET with an in-house topology simulator based on the multi-level-set method and the effect of the thin Si separator is investigated with the simulation results.

MULTI-LEVEL-SET METHOD IMPLEMENTATION

In the multi-level-set method, several materials are represented by the multiple level-set function. In the method, the upper level-set contains the lower level-set and the topology change over time is calculated based on the top level-set function [3]. The surface velocity of top level-set is determined as the surface velocity of the exposed material, as shown in Fig. 1. Since the boundary of the material is extracted unsuitably for the device representation with the corresponding level-set function alone, the boundary extraction is performed by considering not only the corresponding layer level-set but also the lower layer level-set for the proper boundary extraction, as shown in Fig. 2 (a). And, since time evolution scheme of the multi-level-set method may generate the unphysical thin layer, the thin layer correction scheme is employed for accurate boundary representation, as shown in Fig. 2 (b).

SIMULATION RESULT

The BDI process is simulated with the relevant process flow reported in [2]. The flow of the BDI process is shown in Fig. 3 and Fig. 4. The simulation has been conducted for the processes without the Si separator and with the Si separator, which are shown in Fig. 3 and Fig. 4, respectively. In the case without the Si separator, the $Si_{0.8}Ge_{0.2}$ sacrificial layer is etched with a sloped profile during the $Si_{0.5}Ge_{0.5}$ release process due to its low selectivity (7:1), which could cause difficulty in the gate contact formation process. It can be addressed by introducing a Si separator protecting the $Si_{0.8}Ge_{0.2}$ layer during the release process [2]. The case with the Si separator is represented in Fig. 4. In the process, it is seen that the $Si_{0.8}Ge_{0.2}$ layer exhibits a flat profile owing to the Si separator layer that has a high selectivity to $Si_{0.5}Ge_{0.5}$.

CONCLUSION

In conclusion, the BDI process of the FSFET has been simulated by using our in-house topology simulator based on the multi-level-set method. In the simulation, the effect of Si separator was successfully investigated and the results suggest that this method could be useful in the design of 3D logic device processes.

ACKNOWLEDGMENT

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REFERENCES

[1] H. Mertens et al., *Forksheet FETs for Advanced CMOS Scaling: Forksheet-Nanosheet Co-Integration and Dual Work Function Metal Gates at 17nm N-P space,* Symposium on VLSI Tech., pp. 1-2 (2021)

[2] H. Mertens et al., *Forksheet FETs with Bottom Dielectric Isolation, Self-Aligned Gate Cut, and Isolation between Adjacent Source-Drain Structures,* IEDM Tech., pp. 23-1 (2022)

[3] O. Ertl et al., *A Fast Level Set Framework for Large Three-Dimensional Topography Simulation,* Comput. Phys. Commun. 180, pp. 1242-1250 (2009)

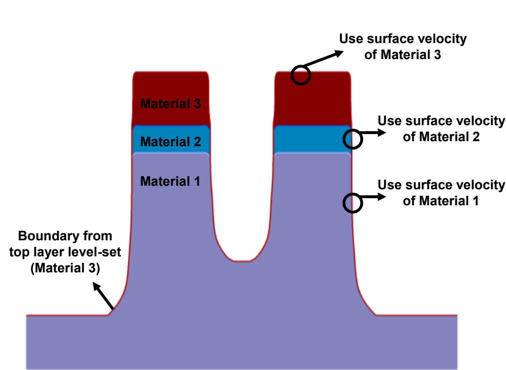

Fig. 1. Schematic of the multi-level-set method. It is shown in which surface velocity is used in the time evolution based on the top layer level-set.

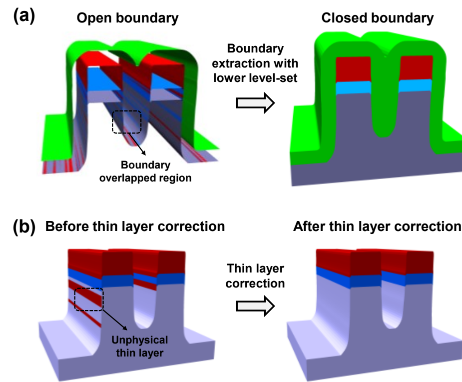

Fig. 2. (a) Closed boundary extraction based on the multiple level-set functions. (b) Correction of a unphysical thin layer.

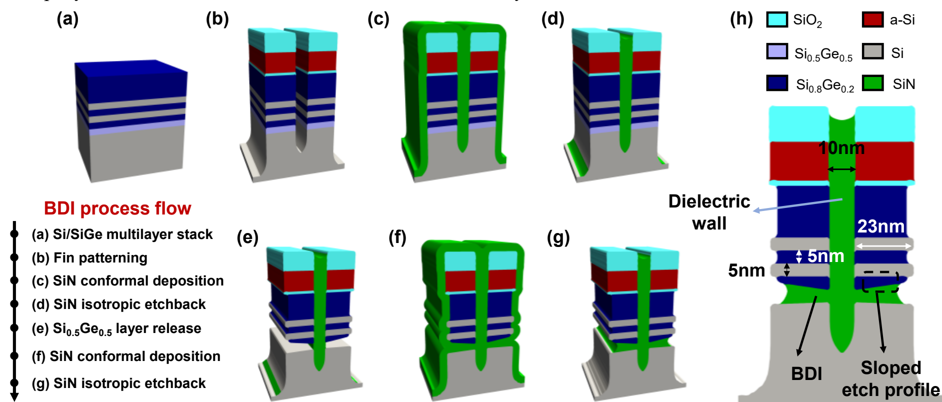

Fig. 3. (a)-(g) The BDI process simulation about the device without the Si separator. The process simulation was conducted by following the represented process flow. (h) Cross section of the simulated device structure.

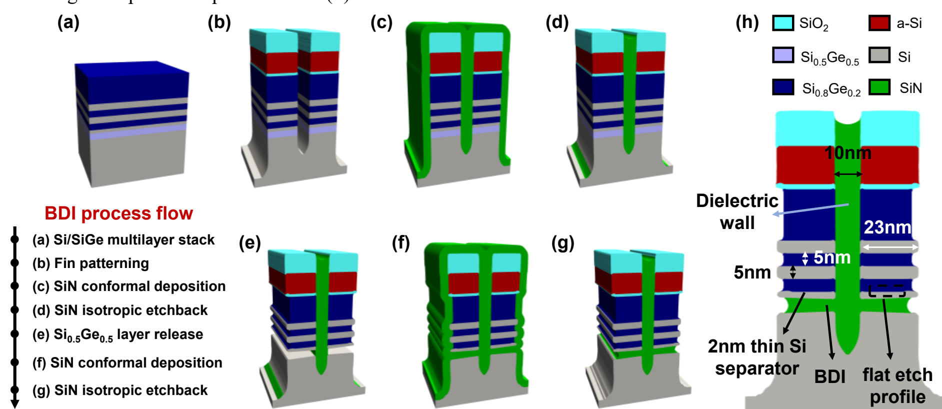

Fig. 4. (a)-(g) BDI process simulation about the device with the Si separator. The process simulation was conducted by following the represented process flow. (h) Cross section of the simulated device structure.