Simulation of ballistic spin-MOSFET devices with ferromagnetic channels

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Newly emerged materials from the family of Heusler alloys and complex oxides exhibit finite bandgaps and ferromagnetic behavior with Curie temperatures much higher than room temperature. In this work, using the semiclassical top-of-the-barrier FET model [1], and a spin dependent contact resistance model derived from [2] (Fig. 2), we explore the operation of a spin-MOSFET that utilizes such ferromagnetic semiconductors as channel materials, in addition to ferromagnetic source/drain contacts (Fig. 1) [3]. Such a device could retain the spin polarization of injected electrons, the loss of which limits the operation of traditional spin transistors with non-ferromagnetic channels, such as Si-spin MOSFETs [4].

We examine the operation of four material systems that are currently considered as some of the most prominent known ferromagnetic semiconductors, three Heusler-type alloys (Mn_2CoAl, CrVZrAl, CoVZrAl) and one from the oxide family ($NiFe_2O_4$) [5]. Importantly, a ferromagnetic semiconductor Heusler alloy has been recently verified [6]. We describe the band structures by using data from DFT calculations, but also consider the effect of 2D confinement in the bands. We investigate under which conditions high spin polarization and significant I_{ON}/I_{OFF} ratio, two essential requirements for the spin-MOSFET operation, are both achieved. We show that these particular Heusler channels, in their bulk form, do not have adequate bandgap to provide high I_{ON}/I_{OFF} ratios, and have small magneto-conductance compared to state-of-the-art devices (Fig. 3). However, with confinement into ultra-narrow sizes down to a few nanometers, and by engineering their spin dependent contact resistances, the proposed geometry can reach 10^3 I_{ON}/I_{OFF} ratio and MR of tens of percentage units (Fig. 3-6). Thus, they could prove promising channel materials for the realization of spin-MOSFET transistor devices that offer combined logic and memory functionalities [3, 4]. Although the main compounds of interest in this paper are Mn_2CoAl, CrVZrAl, CoVZrAl, and $NiFe_2O_4$ alone, we expect that the insight we provide is relevant to other classes of such materials as well.

[1] A. Rahman et al., IEEE Trans. Electron Devices 50, 1853 (2003). [2] T. Valet and A. Fert, Phys. Rev. B 48, 7099 (1993). [3] T. Marukame et al., International Electron Devices Meeting (IEDM) 2009, pp. 1–4. [4] M. Ishikawa et al., J. Magn. Soc. Jpn. 44, 56 (2020). [5] P. Graziosi and N. Neophytou, J. Appl. Phys. 123, 084503 (2018). [6] G. M. Stephen et al., J. Appl. Phys. 125, 123903 (2019).

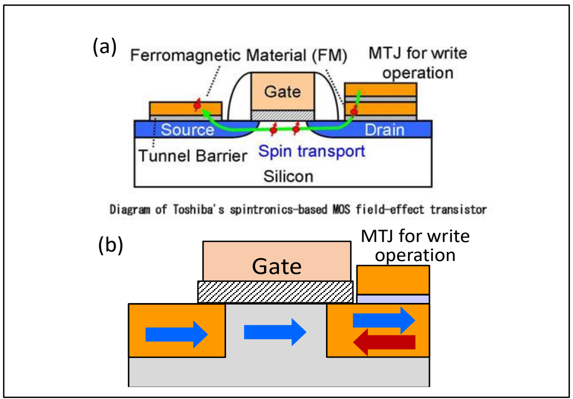

Fig.1: Device schematic of (a) the traditional spin MOSFET concept presented in [3], and the proposed geometry where the channel is composed of a ferromagnetic semiconductor to retain the spin polarization (SP). The arrows indicate the magnetization direction. The drain magnetization can be switched (blue to red and reversely).

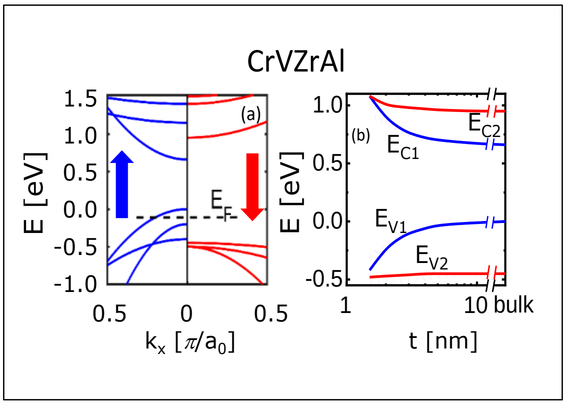

Fig.4: Quantum confinement on the band structure in the Heusler alloy CrVZrAl (a) and shift of the band edges with confinement (b) using parabolic approximation (solid lines) or numerical bands, courtesy of M. Tas, (dashed lines). $E_{C1/2}$, $E_{V1/2}$ are the majority and minority conduction and valence bands edges, respectively.

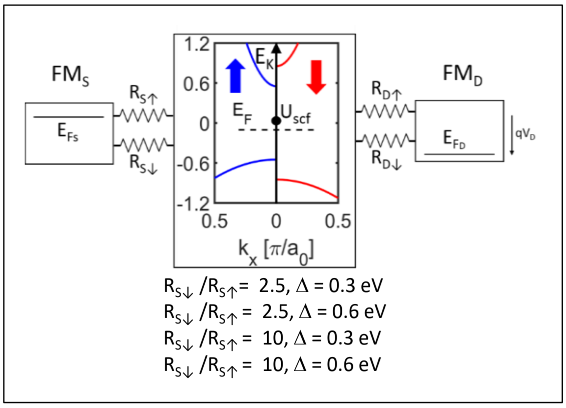

Fig.2: The spin-MOSFET model with spin dependent series resistances introduced for the majority and minority spin carriers at the source/drain contacts. The studied values for the ratio of the majority and minority spin resistances are indicated, with the $R_\uparrow$ = 10^5 Ω. The device is symmetric so that the resistances at source and drain have the same values.

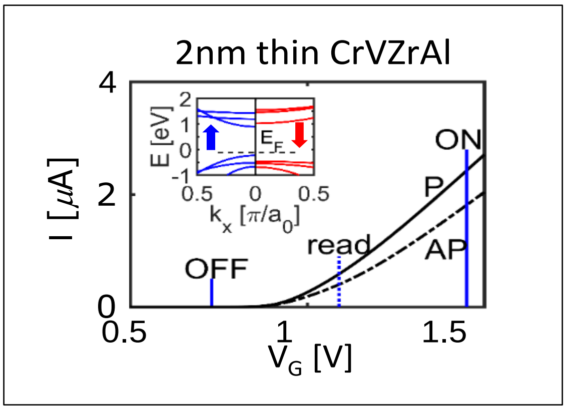

Fig.5: I_D-V_G for a 2 nm narrow CrVZrAl Heusler alloy channel with parallel (P) and anti-parallel (AP) configurations, solid and dashed-dotted lines, respectively. The vertical solid blue lines show V_G^{OFF} and V_G^{ON} for which a ~10^3 I_{ON}/I_{OFF} ratio is achieved at a bias window $V_G = V_D = 0.75$ V for both magnetic configurations. The vertical dotted blue line represents the "read" gate bias V_G^{read} for memory operation.

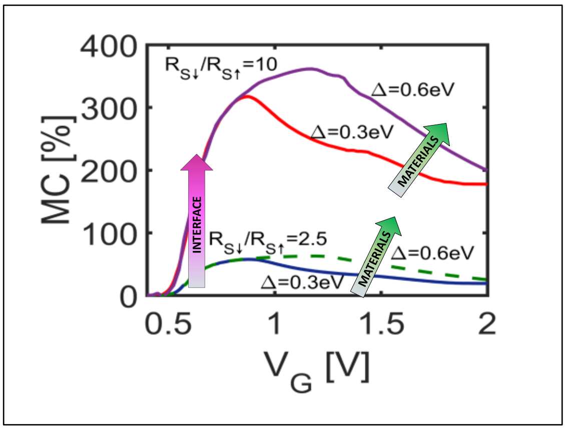

Fig.3: The magnetoconductance (MC) percentage as a function of V_G for V_D = 0.75 V for some parameter combinations as indicated, which shows separately the effect of the spin sub-bands separation Δ and $R_\uparrow/R_\downarrow$ on the MC. The arrows indicate the directions of improvement by engineering the material for Δ or the interfaces for the contact resistances.

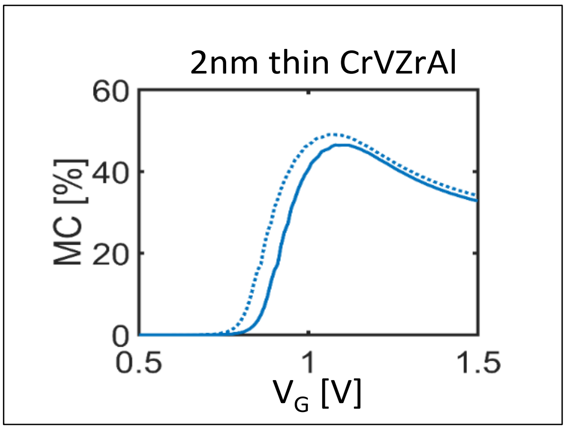

Fig.6: MC versus V_G for the case reported in Fig. 5. The dotted line represents the MC when considering non-parabolicity effects, which increase the MC while the I_D-V_G is only slightly affected.