Deep Learning-Supported Gate-Structure Design for a High Performance Graphene FET

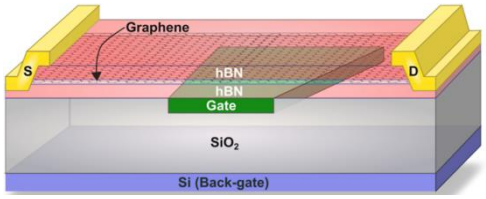
Gyeong Min Seo, and Byoung Don Kong
Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, Republic of Korea
seogm@postech.ac.kr

Graphene field effect transistors (GFETs) are a promising candidate for high-speed radiofrequency (RF) devices due to its high carrier mobilities. However, due to graphene's zero bandgap, the drain current saturation in GFETs that requires a depletion region is not formed. To induce the drain current saturation without opening the bandgap, graphene pseudo optics at p-n junctions, a concept of utilizing the inherent massless Dirac fermion property, was proposed [1]. In this approach, a trapezoidal gate (Fig.1a), designed to reflect the ballistic electrons and suppress Klein tunneling, plays the role of the energy bandgap and a depletion region. Fig.1b represents the saturated drain current of GFET with the trapezoidal gate.

Conventional inverse design method is an iterative optimization. For a defined gate structure of GFET, Id-Vd curve can be calculated by substituting transmission coefficient obtained from graphene finite-difference-time-domain simulation [2] into Landauer equation. The calculated Id-Vd curve is compared to the desired Id-Vd curve, and a little structure change can be applied. This iterative method is time consuming and requires exhaustive numerical simulation for every iteration. In contrast to the iterative optimization approach, deep learning (DL) and deep neural network (DNN) approach is not only able to predict the graphene pseudo-optic response of a specific gate structure of GFET, but is also able to handle the inverse design, providing an optimized gate structure for a targeted graphene pseudo-optic response.

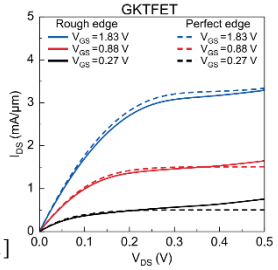
Here, by utilizing the power of deep learning (DL), we report the possibility of discovering a novel design of the gate that maximizes cutoff frequency of GFET. Fig.2 illustrates a tandem architecture [3] for inverse design. A DNN was trained to discover the relation between the gate structure and the graphene pseudo-optics, and to design an optimized gate structure for an improved RF performance. Fig.3 represents a gate structure designed by the DNN and the saturated Id-Vd curve by the DNN-supported gate structure. To conclude, our study suggests that the RF performance of GFETs can be improved by a DNN-supported inverse design. Furthermore, the DNN-supported inverse design can be extended to a different design goal such as maximizing the on/off ratio for a logic device.

[1] Tan, Y et al., *Sci. Rep.* **7**, 9714 (2017)
[2] M.S. Jang et al., *Appl. Phys. Lett.* **97**, 043504 (2010)
[3] D. Liu et al., *ACS photonics*. **5**, 1365 (2018)



Ref. [1]

(a)



Ref. [1]

(b)

Fig. 1: (a) A trapezoidal gate designed to reflect the ballistic electrons and suppress Klein tunneling. (b) The saturated drain current of GFET with the trapezoidal gate.

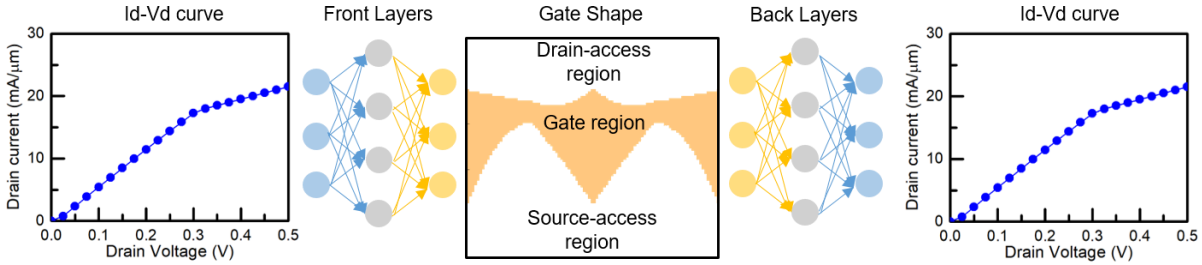
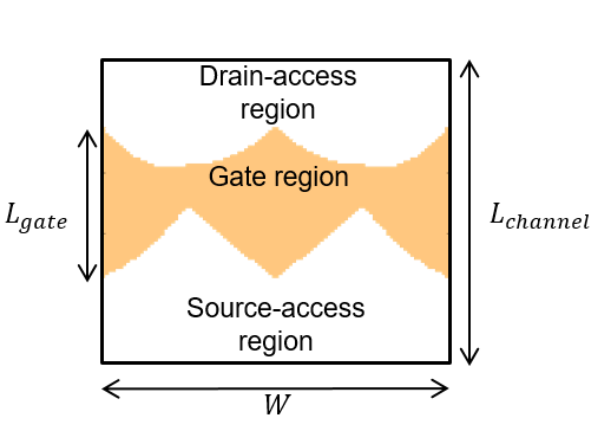
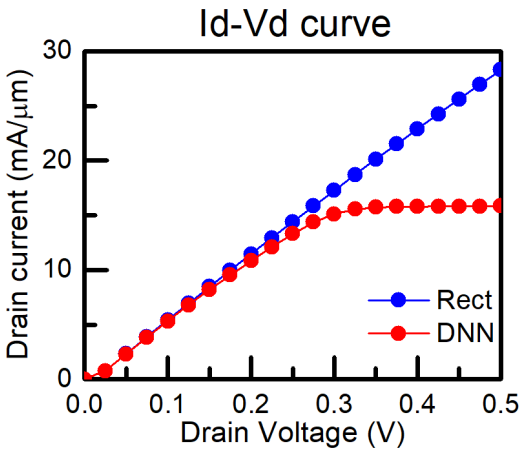


Fig. 2: A tandem architecture for inverse design of gate structure of GFET. Back layers were trained at first, and then front layers would be trained with fixed weights of back layers. After training, DNN of front layers designed an optimized gate structure corresponding to the desired Id-Vd curve.



(a)



(b)

Fig. 3: (a) A DNN-designed gate structure. (b) Id-Vd curve of conventional (rectangular gate) GFET (blue line) and GFET with DNN-designed gate structure (red line).

Parameters:

$V_{top} = 0.1V, V_{bottom} = 50V$, top dielectric: HfO_2(5nm), bottom dielectric: SiO_2(90nm), $L_{channel} = 1\mu m, L_{gate} = 0.5\mu m, W = 1\mu m$