Efficient Machine-learning-based Optimization of 3-nm Node Nanosheet FETs

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Advanced nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs) exhibit short-channel effects (SCE), quantum mechanical effects (QME), and self-heating effects (SHE), which means that design of them requires complex modeling and analysis. Recently, several works have employed machine-learning (ML) techniques and data-intensive neural networks (NN) to model the complex relationships and optimize devices [1]. The Bayesian optimization (BO) has been adopted to realize ML-based data-efficient optimization of MOSFET device, as it requires only a small number of training data in finding the global optimum. However, the previous works used a preset number of iterations (ex. 100 iterations) for the stopping condition [2], which deteriorates efficiency and reliability of BO. Therefore, an effective stopping condition (ESC) which enhances efficiency and reliability of BO needs to be explored. In this work, we constructed a ML-based MOSFET optimization framework (Fig. 1) and investigated ESC by using 2,800 single-gate n-type MOSFETs simulation data (Fig. 2). The data consist of subthreshold swing (SS) and ON-state current with 5-dimensional device specifications. We utilized the maximum expected improvement (EI_{max}) scheme to explore the ESC [3] and stopped BO when EI_{max} are less than 1% of unit value. Our ESC greatly increases the efficiency of BO since it reduces training data up to 87.6% compared to the previous works (Figs. 3(a)-(c)). Our scheme is reliable since the global optimum can be reached before stopping (Figs. 3(d)-(f)). As an application of our ESC scheme to a practical problem, we have optimized a 3-nm node nanosheet (NS) FET in a 5D design space considering QME, SCE, and SHE using a 3D TCAD simulatior (Fig. 4). RC delay, SS, and ON-state maximum temperature were minimized by multi-objective optimization which required small number of training data (<100). Our ML-based optimized 3-nm NSFET exhibits superior performance (22% faster) than human-based optimized one [4] (Fig. 5).

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[1] MH. Oh et al., IEEE Electron Device Lett. 41, 1548-1551 (2020)
[2] W. Lyu et al. PMLR, vol. 80, pp. 3306-3314 (2018)
[3] V. Nguyen et al. PMLR, vol.77 pp. 279-294 (2017)
[4] H. Kim et al. IEEE Trans. Electron. Devices. 67, 1537-1541 (2020)

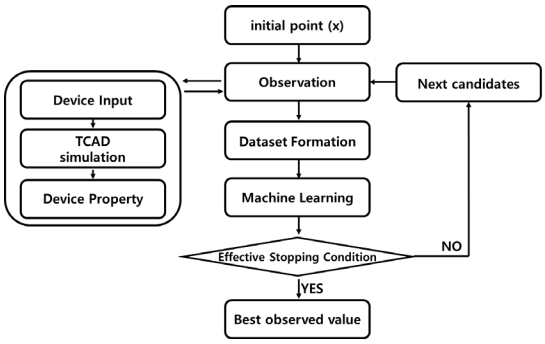
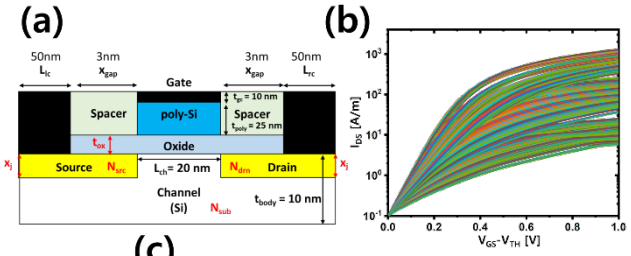


Fig. 1. ML-based MOSFET optimization framework



design variable	values
t_{ox} [nm]	1, 1.5, 2, 2.5, 3
N_{sub} [cm^{-3}]	$10^{11}, 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16}, 10^{17}$
x_j [nm]	1, 1.5, 2, 2.5, 3
N_{src} [cm^{-3}]	$10^{18}, 10^{19}, 10^{20}, 10^{21}$
N_{drn} [cm^{-3}]	$10^{18}, 10^{19}, 10^{20}, 10^{21}$
Total	$5 \times 7 \times 5 \times 4 \times 4 = 2,800$ *devices*

Fig. 2. (a) Device schematics, (b) I-V characteristics, and (c) 5D design space for 2800 single-gate n-type MOSFETs

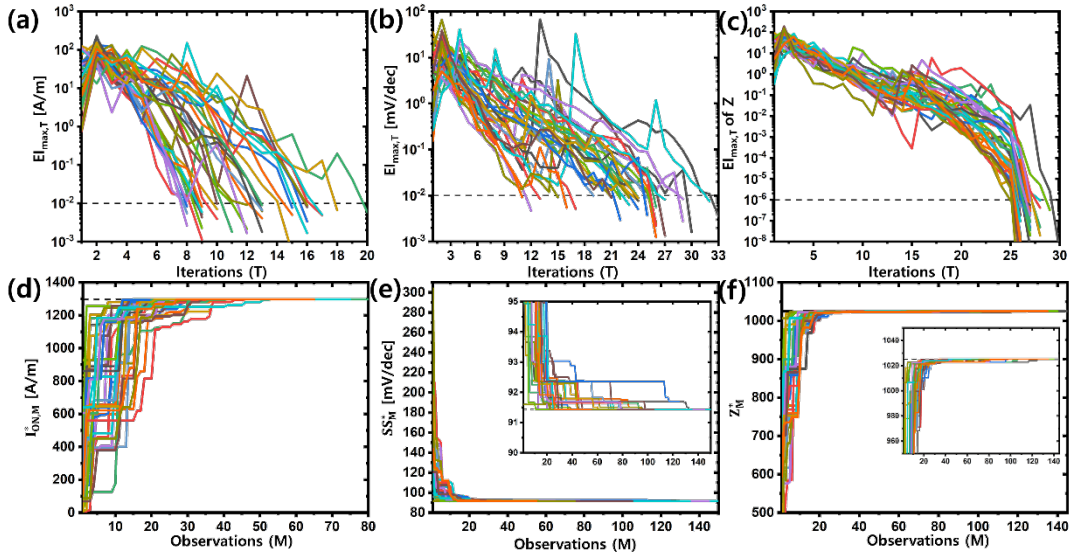
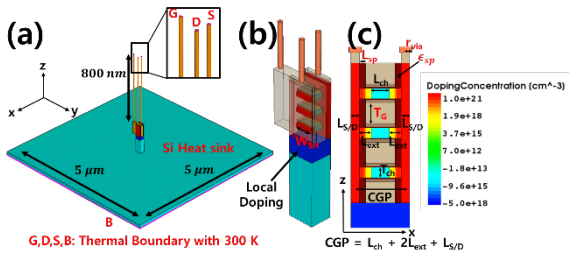


Fig. 3. Efficiency and robustness of ESC scheme. EI_{max} at T iteration for the cases of (a) ON-state current (I_{ON}), (b) SS, and (c) multi-objective function Z are drawn. 12.4, 23.1, and 27.4 iterations were required for optimization on average. The best value at M observation for (d) I_{ON}, (e) SS, and (f) Z are depicted. 34 different sampling seeds were used and every simulation converged to the global optimum.



Design Variable	Values (min, max, interval)
Lsp [nm]	(3,0, 7.0, 0.5)
WSH [nm]	(8.0, 40.0, 1.0)
TG [nm]	(2.0, 20.0, 1.0)
rvia [nm]	(3.0, 7.0, 0.5)
ϵ_{sp} [ϵ_0]	1.0 (Air), 3.9 (SiO_2), 7.5 (Nitride), 22.0 (HfO_2)
Total	9 x 33 x 19 x 9 x 4 = 203,148 devices

Fig. 4. (a) 3D NSFET structure with the thermal boundaries, (b) enlarged device region, (c) x-z plane view at y = 0, (d) 5D design space

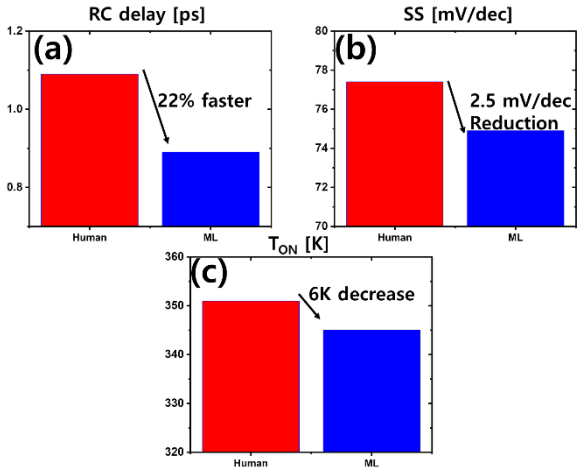


Fig. 5. A comparison between human-based [4] and ML-based optimization. The ML-based optimized device exhibits 22% faster speed, 2.5 mV/dec smaller SS, and 6K lower ON-state temperature than human-based optimized device.