

Efficient 3D 'Atomistic' Simulation Technique for Studying of Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Decanano MOSFETs

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A 3D 'atomistic' simulation technique to study random dopant induced threshold voltage lowering and fluctuations in sub 0.1 μm MOSFETs is presented. It allows statistical analysis of random impurity effects down to the individual impurity level. Efficient algorithms based on a single solution of Poisson's equation, followed by the solution of a simplified current continuity equation are used in the simulations.

1. Introduction

It is widely accepted that random dopant induced parameter fluctuations may limit the MOSFET scaling and integration [1] into decanano dimensions. Several analytical models with different degrees of complexity, describing the random dopant induced threshold voltage fluctuations in MOSFETs, have been developed over the years [2]. Two dimensional numerical simulations have also been used to study, to some extent artificially, the effects of random dopant fluctuations in devices with a channel length down to 100 nm [3]. It is however clear that the detailed study of effects associated with the number fluctuations and the microscopic random distribution of the dopant atoms in decanano MOSFETs requires 3D simulations with fine grain discretization on a statistical scale. This is a computationally demanding task and very few 3D 'atomistic' simulation studies of random dopant fluctuation effects in MOSFETs have been published until now [4, 5].

In this paper we present an efficient methodology for 3D 'atomistic' simulation of random dopant induced threshold voltage lowering and fluctuations in sub 100 nm MOSFETs on a large statistical scale, involving samples of hundreds and thousands of microscopically different devices. Bearing in mind that the computing power, typically available today, is still insufficient for carrying out 3D 'atomistic' simulations even in a conventional drift-diffusion context, our analysis is restricted to low drain voltage and is based on a single 3D solution of the nonlinear Poisson's equation. Using this approach we examine various aspects of the design of random dopant fluctuation resistant MOSFET.

2. Simulation technique

At low drain voltage there is no significant coupling between the current flow and the potential distribution in the MOSFET and the current can be extracted from the solution

of the nonlinear Poisson's equation only. In order to resolve the effects associated with random discrete dopants down to an individual dopant level in decanano devices, a uniform grid with a mesh spacing h typically 1 nm is used in the solution of the 3D Poisson's equation. The average number of dopants in the channel region is calculated by integrating the continuous doping distribution within it. The actual number of dopants in the region is chosen from a Poisson distribution with a mean equal to the calculated average dopant number. Dopants with a probability distribution corresponding to the continuous doping distribution are placed randomly in the random dopant region using a rejection technique. They are assigned to the nearest point of the grid, introducing a charge density q/h^3 .

The Poisson equation at a particular gate voltage is solved for a zero voltage applied between the source and the drain. Then, in the case of an n-channel MOSFET for example, the current density J_n associated with low applied drain voltage V_D is calculated by solving the continuity equation $\nabla \cdot J_n = 0$ with $J_n = \sigma_n E_V$ where σ_n is the local conductivity and E_V is the electric field associated with the applied drain voltage. This leads to the following elliptic equation for the potential V driving the current:

$$\nabla \cdot \mu_n n \nabla V = 0 \quad (1)$$

where μ_n is the electron mobility and n is the electron concentration calculated from the solution of the Poisson's equation. For properly scaled MOSFETs it is usually enough to solve Eq. (1) in a solution domain extending from the Si/SiO₂ interface down to less than 10 nm in the semiconductor. The boundary conditions are: $V = 0$ at the source contact, $V = V_D$ at the drain contact, and zero normal derivative of V at all other boundaries of the solution domain. In contrast to the standard drift-diffusion equation,

the discretization of Eq. (1) leads to a symmetrical positive definite matrix which can be solved using standard iterative techniques.

The sharp variations in the potential resulting from the discrete nature of the charges on short length scales have an adverse effect on the convergence of most iterative solvers. We have developed a multigrid solver for the solution of the Poisson and current continuity equations. It is very efficient, reducing both the long range residual components associated with the boundary conditions and the short range residual components associated with the discrete dopants in one W iteration cycle [6].

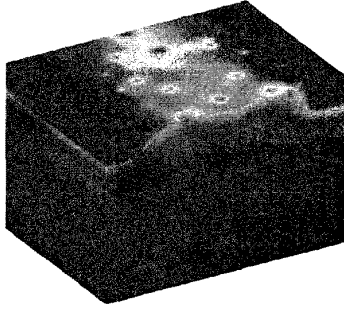


Fig. 1 Potential distribution in a 50x50 nm channel MOSFET with doping concentration in the channel region $N_A = 5 \times 10^{18} \text{ cm}^{-2}$ and oxide thickness $t_{ox} = 3 \text{ nm}$.

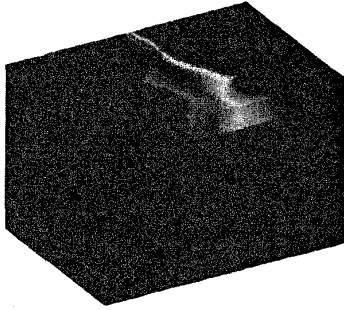


Fig. 2. Distribution of the potential V driving the current along the channel in the MOSFET from Fig. 1, obtained from the solution of the modified current continuity equation (1).

Fig. 1 illustrates a typical potential distribution in a 50x50 nm channel MOSFET with doping concentration in the channel region $N_A = 5 \times 10^{18} \text{ cm}^{-2}$ and oxide thickness $t_{ox} = 3 \text{ nm}$. The average number of dopants in the channel depletion region of the above transistor is 170. The distribution of the potential V driving the current along the channel and obtained from the solution of the modified current continuity equation (1) is given in Fig. 2.

3. Conventional MOSFET

In this section we present results for MOSFETs with conventional architecture and uniform doping concentration

in the channel depletion region. The dependence of the threshold voltage as a function of the number of dopant in the channel depletion region for 2500 microscopically different 50x50 nm MOSFETs with doping concentration in the channel region $N_A = 5 \times 10^{18} \text{ cm}^{-2}$ and oxide thickness $t_{ox} = 3 \text{ nm}$ is plotted in Fig. 3. The correlation coefficient between the number of dopants in the channel depletion region and the threshold voltage is 0.67. It is clear that not only the total number fluctuations but also the individual random placement of dopants in the depletion region have significant contribution to the threshold voltage fluctuations.

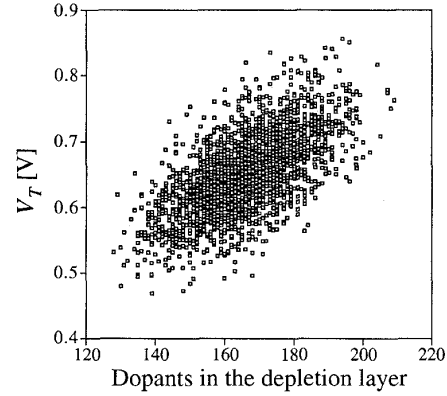


Fig. 3.

Threshold voltages in a sample of 2500 microscopically different 50x50 nm MOSFETs as a function of the number of dopants in the depletion layer. $N_A = 5 \times 10^{18} \text{ cm}^{-2}$ and $t_{ox} = 3 \text{ nm}$.

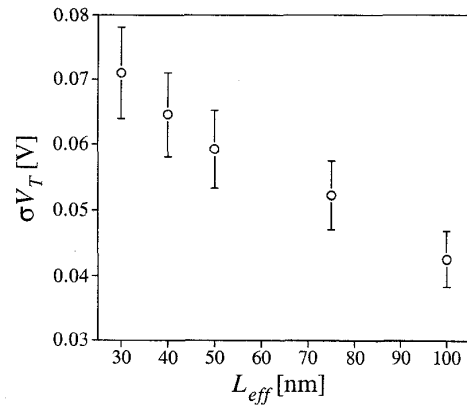


Fig. 4 Standard deviation in the threshold voltage σV_T as a function of the effective channel length L_{eff} for a set of MOSFETs with $W_{eff} = 50 \text{ nm}$, $N_A = 5 \times 10^{18} \text{ cm}^{-2}$ and $t_{ox} = 3 \text{ nm}$. Samples of 200 transistors.

Fig. 4 gives an impression for the magnitude of the threshold voltage standard deviation σV_T in sub 0.1 μm MOSFETs with 50 nm channel width, different channel lengths and conventional architecture. The predicted σV_T of more than 60 mV for transistors with $L_{eff} = 50 \text{ nm}$ is totally unacceptable for the corresponding systems with more than one billion transistors on chip and supply voltage less than

1 V. According to the current level of understanding [2] the threshold voltage fluctuations in MOSFETs with conventional architectures increase with the doping concentration in the channel as shown in Fig. 5.

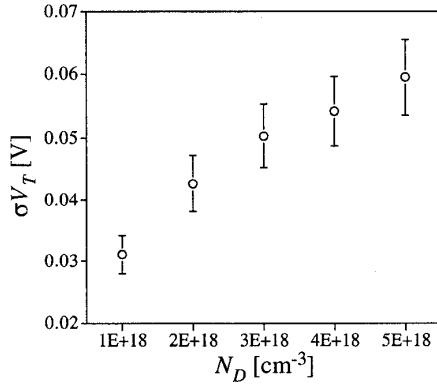


Fig. 5. Standard deviation in the threshold voltage σV_T as a function of the doping concentration N_A in MOSFETs with $L_{eff} = 50$ nm, $W_{eff} = 50$ nm and $t_{ox} = 3$ nm. Samples of 200 transistors.

The 'atomistic' simulation predicts lower average threshold voltage compared to the threshold voltage obtained from the simulation of analogous MOSFETs with continuous doping distribution. This threshold voltage lowering is associated with a current percolation through the potential fluctuations at the surface, introduced by the random dopants. As shown in Fig. 6 the threshold voltage lowering rapidly increases with the reduction of the channels length.

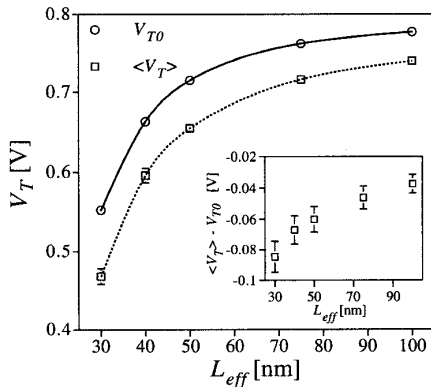


Fig. 6. Threshold voltage and threshold voltage lowering as a function of the channel length for MOSFETs with $W_{eff} = 50$ nm, $N_A = 5 \times 10^{18} \text{ cm}^{-2}$, and $t_{ox} = 3$ nm. Samples of 200 transistors.

For devices with a constant channel length the threshold voltage lowering increases with the channel width as indicated in Fig. 7 and may reach 0.1 V in a MOSFET with $L_{eff} = 50$ nm and $L_{eff} = 400$ nm. The grid associated with the 'atomistic' simulation of the latest device contains 1,400,000 nodes. The threshold voltage lowering in decanano MOSFETs may compensate partially the increase in the

threshold voltage associated with the quantisation in the surface depletion layer.

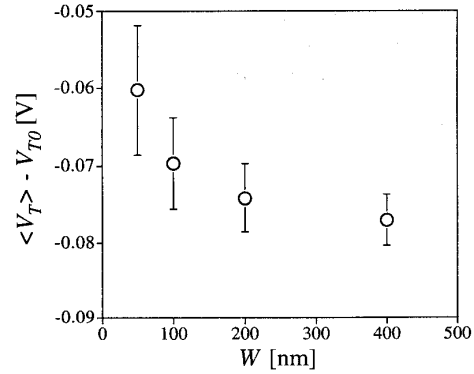


Fig. 6. Threshold voltage lowering as a function of the channel width for MOSFETs with $L_{eff} = 50$ nm, $N_A = 5 \times 10^{18} \text{ m}^{-2}$ and $t_{ox} = 3$ nm. Samples of 200 transistors.

4. Fluctuation resistant MOSFETs

Due to the limitations of the conventional MOSFETs discussed above the development of random dopant fluctuation resistant device architectures is becoming an important area of research. It has been demonstrated that the introduction of a low doped epitaxial layers in channel engineered MOSFET can substantially reduce the random dopant induced threshold voltage fluctuations [7], enhancing in the same time the channel mobility. Fig. 8 illustrates the reduction of σV_T with the increasing thickness of the undoped epitaxial layer in a 50x50 nm MOSFET.

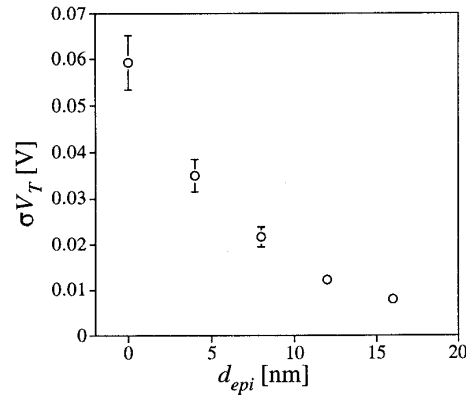


Fig. 8. Standard deviation in the threshold voltage σV_T as a function of the thickness of the epitaxial undoped channel layer d_{epi} for a set of MOSFETs with $L_{eff} = 50$ nm, $W_{eff} = 50$ nm, $N_A = 5 \times 10^{18} \text{ cm}^{-3}$, and $t_{ox} = 3$ nm. Samples of 200 transistors.

The dependence of σV_T on the doping concentration is illustrated in Fig. 9 for a set of MOSFETs with different thickness of the epitaxial layer. In contrast to the conventional MOSFETs in epitaxial architecture both

increase and decrease of σV_T with the doping concentration can be observed depending on the thickness of the epitaxial layer. In MOSFETs with thick epitaxial layers the width of the depletion region is small and the mobile majority carrier behind the depletion layer screen the potential fluctuation associated with the random dopants in it.

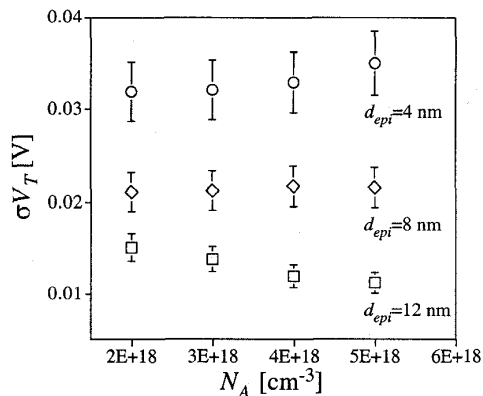


Fig. 9. Standard deviation in the threshold voltage σV_T as a function of the doping concentration N_A in an epitaxial channel MOSFETs with different thickness of the epitaxial layer d_{epi} , $L_{eff} = 50$ nm, $W_{eff} = 50$ nm and $t_{ox} = 3$ nm. Samples of 200 transistors.

The epitaxial channel devices, however, will require an excessively high doping concentration below the epitaxial layer to suppress the 2D short channel effects. This in turn will increase the source/drain capacitances and will reduce the breakdown voltage to unacceptably low levels. A carefully designed δ -doping layer below the epitaxial channel can provide an efficient short channel and threshold voltage control, reducing some of the detrimental heavy doping effects [8].

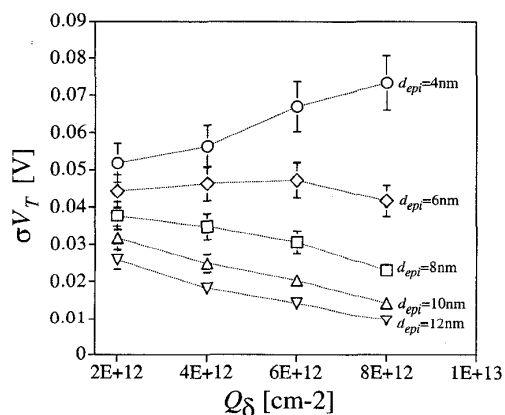


Fig. 10 Standard deviation in the threshold voltage σV_T as a function of the δ -doping concentration Q_δ in an epitaxial δ -doped MOSFETs with various d_{epi} , $L_{eff} = 50$ nm, $W_{eff} = 50$ nm, $N_A = 1 \times 10^{18}$ cm^{-3} and $t_{ox} = 3$ nm. Samples of 200 transistors.

The threshold voltage fluctuation in δ -doped structures can also either increase or decrease with the amount of the delta doping depending on the thickness of the epitaxial layer as illustrated in Fig. 8. In epitaxial layers with intermediate thickness σV_T passes through a maximum as a function of the delta doping sheet concentration. For a thin epitaxial layer the delta doping region is completely depleted and the discrete charge of all dopants there contribute to the threshold voltage fluctuations. For thicker epitaxial layers the carriers in the delta doping region are only partially depleted and screen the potential fluctuations. In this case the screening increases with the δ -doping concentration and reduces further the fluctuations.

5 Conclusions

A simple and efficient algorithm for 3D 'atomistic' simulation of random dopant induced threshold voltage lowering and fluctuations in sub 100 nm MOSFETs has been presented.

The detailed analysis shows that the threshold voltage fluctuations are determined not only by the fluctuation in the dopant number, but also in the individual dopant position.

Due to its efficiency, the presented simulation approach can be used for practical statistical device design and optimisation.

Although the random dopant induced fluctuations reach an unacceptable level in decanano devices with a conventional architecture they can be significantly reduced by using remote and delta-doped channel profiles without drastic change in the MOSFET architecture

References

1. Y. Taur, D.A. Buchanan, W. Chen, D.J. Frank, K.E. Ismail, S.-H. Lo, A.A. Sai-Hakasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind and H.-S. Wong: Proc. IEEE **85** (1997) 486.
2. K. R. Lakshmi Kumar, R.A. Hadaway and M.A. Copeland: IEEE J. Solid State Circ. **SC-21**, (1986) 1057.
3. P.A. Stolk and D.B.M. Klaasen: Proc. IEDM'96. Dig. Tech. Papers (1996).
4. H.-S. Wong and Y. Taur: Proc. IEDM'93. Dig. Tech. Papers (1993) 705.
5. J.-R. Zhou and D.K. Ferry: Proc. 3rd Int. Workshop on Computational Electronics, Plenum Press, New York, (1994) 74.
6. C. R. Arokianathan, J. H. Davies and A. Asenov: VLSI Design, in press.
7. K. Takeuchi, T. Tatsumi, and A. Furukawa: Proc. IEDM'97 Dig. Tech. Papers (1997).
8. K. Noda et al.: IEEE Trans. Electron Devices, **45** (1998) 809.