System simulation tools for single-electronic devices

Scott Roy, John R Barker and Asen Asenov

Nanoelectronics Research Centre
Department of Electronics and Electrical Engineering
University of Glasgow
Glasgow G12 8QQ, UK

Abstract
Single-electronic systems are described by coupled sets of circuit equations which link the charge, voltage and current distributions of tunnelling and non-tunnelling capacitor arrays.The concept of critical charge is used to implement an efficient network solver. System simulation may then be achieved by Monte Carlo methods although this is often prohibitive computationally .Alternatively, linear programme techniques can establish the boundaries for stable operation. The full 3D modelling of the capacitance matrix is required for recently developed Schottky dot structures.

I. Introduction

The recent development of single-electronic devices has exploited the phenomenon of correlated single electron tunnelling[1] in coupled tunnel junctions(ultra-small capacitor arrays) under conditions set by the Coulomb blockade threshold $e^2/2C >> kT$. At least three different classes of structure are currently under study experimentally: vertical metal-insulator-metal[2-4], lateral metal semiconductor metal[5] ; and laterally patterned two-dimensional electron gases in semiconductor heterostructures[6]. These new devices pose new challlenges for computational electronics[7]: they are strongly capacitively coupled, the major transport mechanism is correlated tunnelling, the presence of thermal fluctuations, cross-talk, charge trapping de-trapping and macroscopic quantum tunnelling are all potentially killer effects. Most significantly existing single-electronic systems may be quite large (up to 100 devices) requiring new systems tools for design and analysis.

II. Network solver

We have developed a set of simulation tools based on a similar formalism to Bakhvalov et al[10] for a linear array of tunnel junctions but extended to arbitrary single electron tunnel junction circuit configurations using a matrix representation of the various voltages, currents and circuit elements. The general theory derives from an analysis of a basic tunnelling event and a single tunnel junction (capacitance C) in series with a non-tunnelling capactance C_e and a voltage source V_0. The tunnelling rate Γ is determined by the temperature T and the free energy change following the tunnel event[1]: $\Gamma(\Delta E,T) = (\Delta E/e^2R_t)[\exp(\Delta E/k_BT)-1\}^{-1}$ where R_t is the junction tunnelresistance. At low temperatures

$\Gamma(\Delta E)= (-\Delta E/e^2R_t)$ $(\Delta E<0)$; $\Gamma(\Delta E) = 0$ $(\Delta E<0)$. (1)

For the simple circuit we have: $E = Q_e^2/(2C_e) + Q_c^2/(2C) + Q_vV_0$; where Q_v is the charge through the voltage source and the critical charge $Q_c = e/(2[1+C_e/C])$. For a single electrontunnel event we find

$\Delta E = -eQ/C + e^2/(2(C+C_e))$ (2)

This "instantaneous" model for tunnelling provides a first level for our system simulation tools. A second level utilises the quantum Langevin equation[ ] approach handle fluctuations (due to lack of space we do not describe that here). The critical charge is the charge at which tunnelling becomes advantageous; the critical charges for a circuit depend solely on the junction

capacitance and the lumped capacitance C_{eff} of the remaining circuit. We have developed a network solver for C_{eff} by deploying an impedance matrix **Z**, positive definite with rank equal to the number of loops in the circuit. The diagonal elements are the total impedances around each mesh; the off-diagonal terms are the total impedances shared by two loops. By partitioning this matrix we can separate out loops of no interest to obtain a lower rank effective impedance matrix Z_{eff}. Hence we may determine the critical charges.

III. Monte Carlo and Linear Programming simulators

The Monte Carlo simulator uses the general network solverto find the critical charges for each device for which tunnelling becomes feasible in the tunnel junction network. The simulator then iterates "events" by repeatedly characterising the circuit for a given set of input voltages and clocked charge positions, discovering which tunnelling event will occur next and updating dependent and independent circuit parameters using charge conservation and the circuit matrix equations. Although this approach is important it is computationally expensive especially for the larger extended systems of coupled devices.
To obtain a more rapid assessment of the possible stable operating regimes of single electronic devices and systems we have developed a *linear programming* technique which allows us to determine the allowed regime of stable operation in the control parameter space. The method is essentially an inverse of the Monte Carlo approach: the allowed or disallowed tunnel events are defined first followed by a detrmination of the circuit voltages and charge values. The approach is illustrated in figures 2-4 for a turnstile device[4] shown schematically in figure 1. The Monte Carlo results for the operational area of V_g-V_a space (fig 4) are given by accumulating legal points. The area so-defined is found to be well-modelled by boundary lines determined from linear programming using the tunnel event schematics of figure 3.

These new simulation tools have been used to study effects of cross-talk and inter array coupling in single-electronic systems. Figure 6 shows typical results of the effects of stray capacitance couplin C_{stray} on the current through two parallel tunnel junction arrays shown in figure 5.

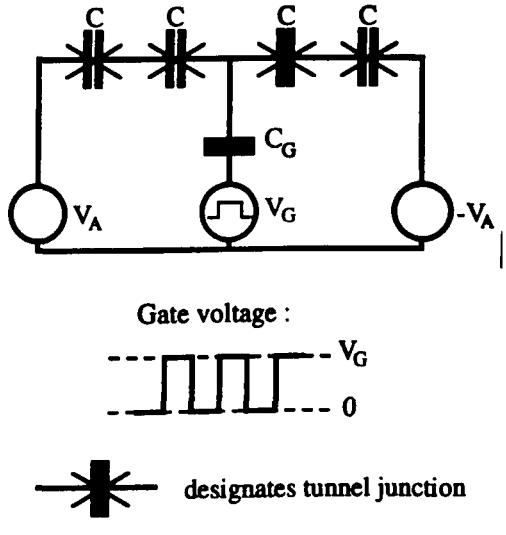

Figure1. 2-phase turnstile device

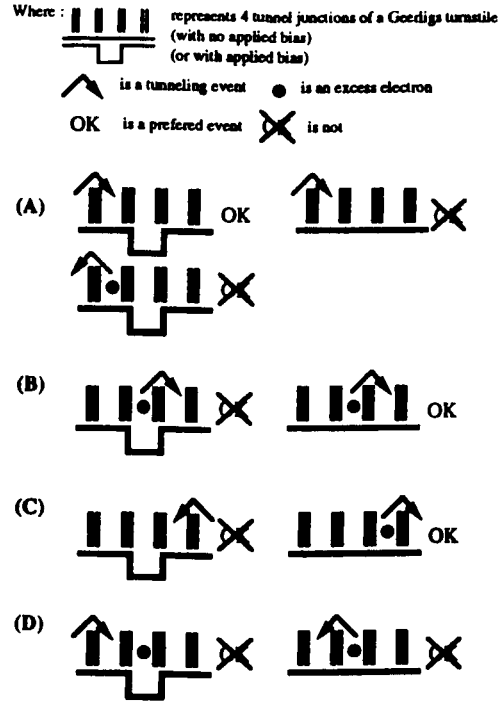

Figure2.Linear programming schematics

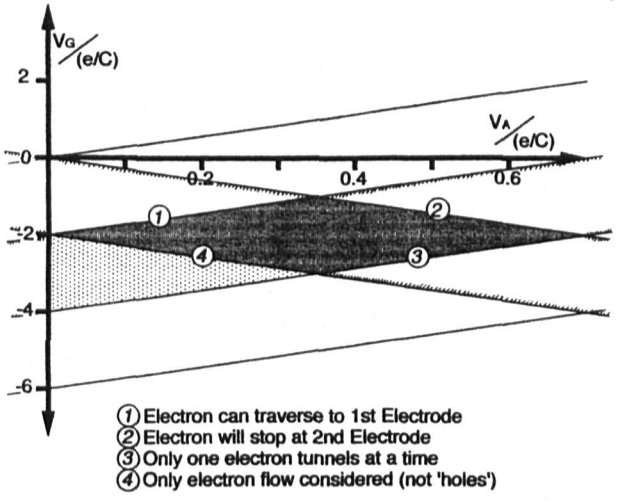

Figure 3. Legal area of turnstiling operation in VG, VA space .Dark shading = safe operation

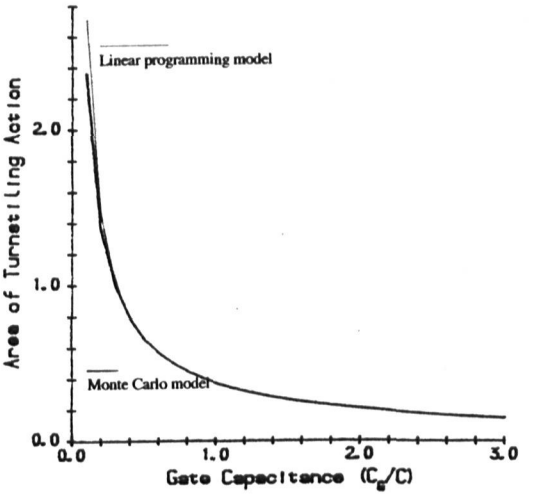

Figure 4. Legal area of turnstiling operation in VG, VA space versus gate capacitance

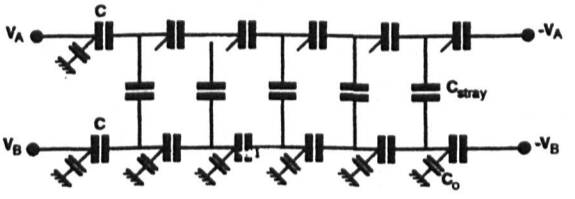

Figure 5. Linked tunnel junction arrays

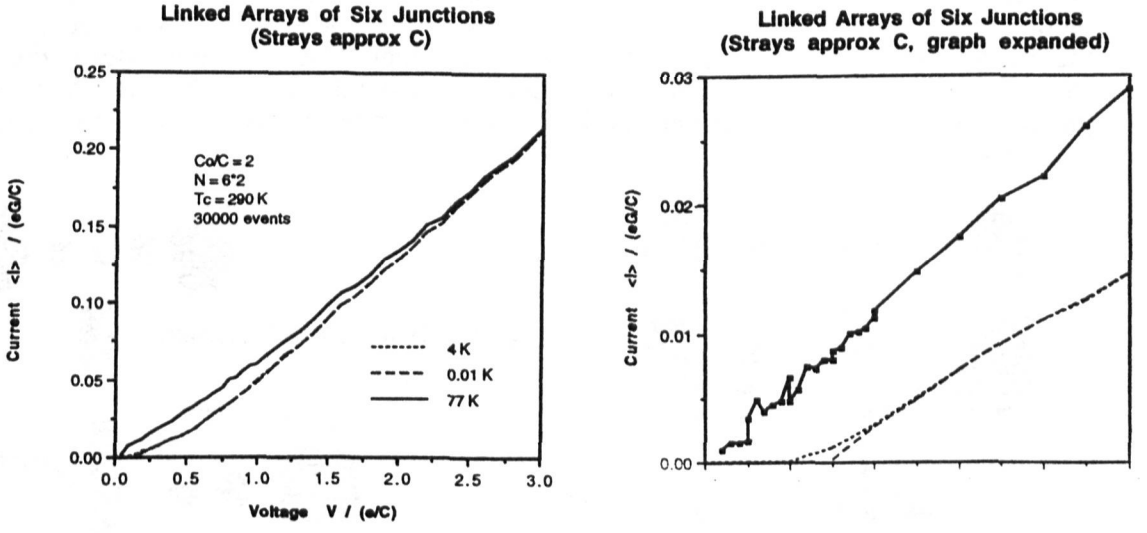

Figure 6. Current-voltage characteristics for Linked tunnel junction arrays

IV. Schottky dot systems

The traditional approach to single-electronic devices has utilised the hanging-resist technology developed for metal-insulator-metal tunnel junctions[2]. Although this method has allowed construction of large numbers of interconnected junctions in complex circuits it is limited by the lithography to relatively large capacitances and consequently very low operating temperatures. Very recently a much finer resolution lithography which has fewer processing stages and involves forming ultra-fine (< 5 nm radii and spacings) metal on semiconductor electrodes, Schottky islands and dot arrays has been developed at Glasgow[5](Fig 7).These new structures involve ultra-small capacitances with equivalent Coulomb blockade temperatures in excess of 60K scaleable to much greater than room temperature. The dot structures may be arranged laterally to form pass transistors (fig8), RAM cells (fig9) or more complex circuits. An essential feature of these systems is the requirement for the "tunnelling tails" of the Schottky islands to overlap thus permitting correlated electron tunnelling from dot to dot via the semiconductor. Modelling of these systems is crucial in order to determine the effective capacitance matrix and for understanding how to control effects of unwanted traps (charge-trapping de-trapping effects) which can destroy single electronic stability.by structuring the substrate, ground planes, doping levels and island geometry.

The develpment of stable and reliable single electronic systems requires the precise design of both the junction capacitances (inter-capacitances) and the capacitances to ground. Since the measurement of such ultra-small capacitances is very difficult experimentally the design becomes reliant on the numerical simulation of the capacitance matrices. The problem is essentially a 3D problem involving complicated geometries, several dielectric regimes, and device physics which involves surface conditions, random distributions of traps and their dynamics.

To illustrate part of the design problem and the importance of an adequate numerical solution we present here some results of 2D simulation of Aluminium wires on the surface of p-silicon as an approximation to the Schottky dot devices shown in Figures 7-9. The simulations were performed by the simulator H2F [8]. Figure 10 shows the potential distribution around two 40 nm width wires with 12 nm spacing. The fringing effects and presence of the silicon substrate increased the junction capacitance 4 times in comparison with the simple parallel plate formula. The ground capacitance is more than twice as high as the junction capacitance. The presence of surface pinning states modifies the picture. The presence of donor type states near the middle of the bandgap increaes the ground capacitance slightly, but a more profound effect is produced by modelling acceptor states which significantly increae the capacitance(25%).The juction and ground capacitances may be tuned by anisotropic etching leaving metal islands on the top of silicon pedestals (figure 11). It is found that 200nm etching reduces the junction capacitance by a factor of 3x and the capacitance to ground is diminished by a factor of 2x. A parallelised 3D simulator is under development for for more realistic prediction and design of such devices[9].

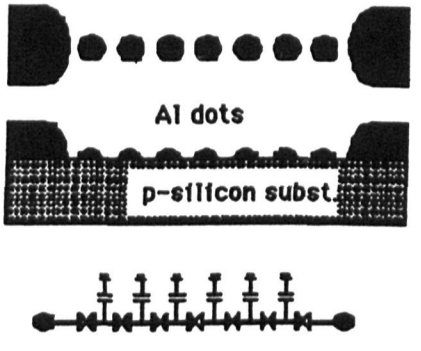

Figure 7. Schematic and equivalent circuit of Schottky dot arrays

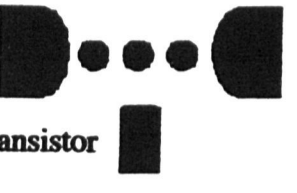

Figure 8. Schottky dot transistor

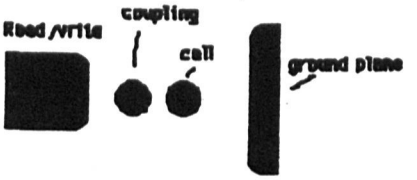

Figure 9 Schottky dot RAM cell

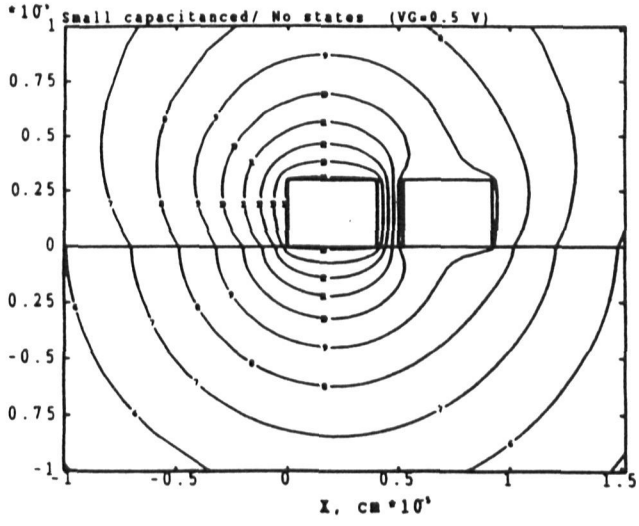

Figure 10. Potential distribution around two Schottky dots on Si.

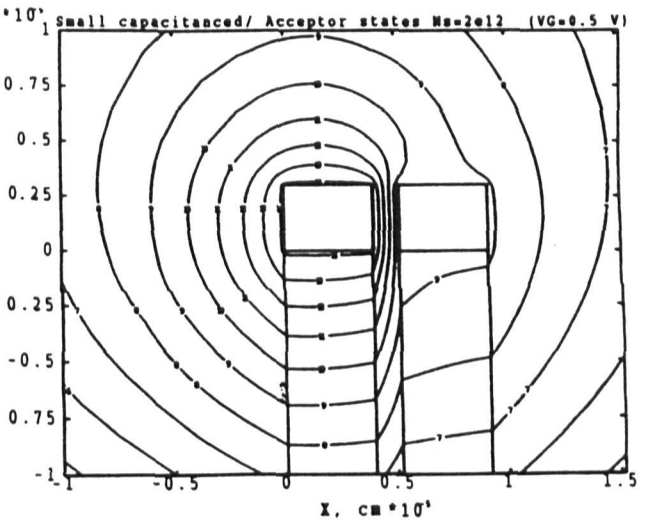

Figure 11. Potential distribution around two Schottky pedestals on Si.V_G =0.5V

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