Boundary Conditions for Quantum Devices with Exposed Surfaces

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Abstract
The purpose of this work is to investigate the boundary conditions for the potential at exposed semiconductor surfaces in split-gate structure. A two dimensional numerical approach is presented for the coupling between the non-linear Poisson equation in the semiconductor (Finite Element Method) and Laplace's equation in the dielectric (Boundary Element Method). The utility of the coupling algorithm is demonstrated by simulating the potential distribution in a $n - AlGaAs/GaAs$ quantum wire structure with a semi-classical Thomas-Fermi charge model.

I. Introduction

Recent advances in nanostructure fabrication have made it possible to fabricate structures in which a two-dimensional layer of electrons is further confined into quantum wires or dots. Typically, such device structures are defined by metallic split gates. In order to understand the potential distribution in those structures, we solve Poisson's equation in the two-dimensional problem domain,

$$\epsilon \nabla^2 \phi = -\rho, \tag{1}$$

where ϕ is the electrostatic potential, ϵ is the dielectric constant, and ρ is the charge density [1]. Since this is a boundary value problem, one needs to know the values of the potentials and/or fluxes at the boundary. This is a crucial problem, especially at the exposed semiconductor surface.

In recent studies [1]-[7], the problem domain is typically identical with the semiconductor region, schematically shown in Fig. 1. The commonly used model for the boundary conditions on the exposed semiconductor surface is either a Dirichlet boundary condition [2],[3] or a Neumann boundary condition [4],[5]. Obviously, both of these models have their limitations, especially for very narrow split-gate structures used for quantum devices.

In this paper, we adopt an alternative viewpoint and develop an algorithm to implement boundary conditions at exposed semiconductor surfaces. We view as the natural problem domain the semiconductor *and* the dielectric, as shown in Fig. 2. Thus the artificial boundary conditions at the exposed surface are replaced by more physical matching

conditions at the interface between the semiconductor and the dielectric. Specifically, this algorithm, referred to as FBEM, couples a Finite Element solution of Poisson's equation in the semiconductor to a Boundary Element solution [8] of Laplace's equation in the dielectric with matching conditions.

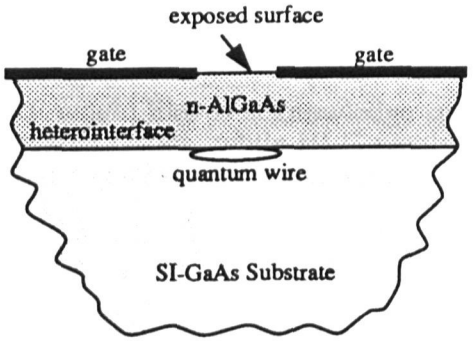

Figure 1: Typical problem domain for quantum devices defined by metallic gates. Shown are the multi-layer semiconductor regions and the exposed surface between the gates.

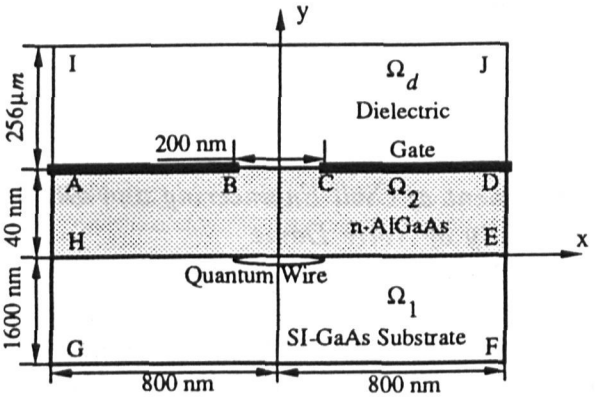

Figure 2: The problem domain consisting of the semiconductor regions, Ω_1 and Ω_2, and the dielectric region, Ω_d. the semiconductor exposed surface B-C is treated as the interface between the semiconductor and the dielectric.

In Section II, we present the problem statement with the formulation of the boundary conditions on the exposed surface. In Section III, we discuss our numerical problem formulation. In Section IV, we present example results of the FBEM calculation for a $n - AlGaAs/GaAs$ quantum wire structure under bias conditions, and we compare them to those obtained with the usual Dirichlet and Neumann boundary conditions.

II. Problem Statement

We solve the two dimensional potential problem in the domain shown in Fig. 2, where regions Ω_1 with boundary $\partial\Omega_1$ and Ω_2 with boundary $\partial\Omega_2$ are semiconductor domains (non-linear Poisson equation) and region Ω_d with boundary $\partial\Omega_d$ is the dielectric domain (Laplace's equation). The simulation variable, u, is defined as the potential difference between the conduction band edge E_C and the Fermi energy E_F in units of the thermal energy kT, i.e., $u \equiv (E_C(\phi) - E_F)/kT = (E_C^b - e\phi - E_F)/kT$, where E_C^b is the conduction band edge in the bulk. The boundary C-B is the exposed semiconductor surface. Mathematically C-B is the interface between the region Ω_2 and the region Ω_d. Across this interface, the potential, u, is continuous and the jump in the normal electric flux density is equal to the interface charge density. The problem to be solved can be posed as follows:

Find:

$$u = u_1,\ u_2,\ u_d, \tag{2}$$

such that

$$\epsilon_l \nabla^2 u_l(x,y) = -f[u_l(x,y)], \qquad (x,y) \in \Omega_l, \qquad l = 1,2, \tag{3}$$

$$\epsilon_d \nabla^2 u_d(x,y) = 0, \qquad (x,y) \in \Omega_d, \tag{4}$$

and with interface matching conditions at the exposed surface, $\partial\Omega_{BC}$:

$$u_2 - u_d = 0, \qquad on\ \partial\Omega_{CB}, \tag{5}$$

$$\epsilon_2 \frac{\partial u_2}{\partial \vec{n}} - \epsilon_d \frac{\partial u_d}{\partial \vec{n}} = \frac{e}{kT} Q_{int}, \qquad on\ \partial\Omega_{CB}, \tag{6}$$

where $f(u_l) = f_l = e\rho(u_l)/kT$, is the charge density term in the domain Ω_l, and Q_{int} is the interface charge density on the interface $\partial\Omega_{CB}$. Generally Q_{int} and ρ may be a function of the potential u, that is, $Q_{int} = Q_{int}(u)$ and $\rho = \rho(u)$.

III. Numerical Formulation

The semiconductor domain Ω_s, $\Omega_s = \Omega_1 \cup \Omega_2$, where the non-linear Poisson equation (3) governs, is discretized in a way suitable for the application of the Finite Element Method (FEM). The resultant non-linear system of equations is:

$$\begin{aligned} \mathbf{K}_{11}\mathbf{u}_o^s + \mathbf{K}_{12}\mathbf{u}_{BC}^s &= \mathbf{p}_f^s, \\ \mathbf{K}_{12}^T\mathbf{u}_o^s + \mathbf{K}_{22}\mathbf{u}_{BC}^s &= \mathbf{p}_{BC}^s, \end{aligned} \tag{7}$$

where $\mathbf{u}_{BC}^s$ and $\mathbf{p}_{BC}^s$ contain the potentials and nodal forces, respectively, at the nodes on the interface $\partial\Omega_{BC}$ between the semiconductor and the dielectric, $\mathbf{u}_o^s$ and $\mathbf{p}_f^s$ contain the potential and nodal forces at all other nodes in the semiconductor domain, respectively, and $\mathbf{K}$ is the stiffness matrix.

The dielectric domain, Ω_d, is a homogeneous charge free region. The governing equation is Laplace's equation. Since the fundamental solution of Laplace's equation (4) is known, a boundary integral equation technique can be employed. The resultant system of equations can be expressed as:

$$\begin{aligned} \mathbf{S}_{11}\mathbf{u}_o^d + \mathbf{S}_{12}\mathbf{u}_{BC}^d &= \mathbf{p}_o^d, \\ \mathbf{S}_{21}\mathbf{u}_o^d + \mathbf{S}_{22}\mathbf{u}_{BC}^d &= \mathbf{p}_{BC}^d. \end{aligned} \tag{8}$$

where $\mathbf{S}^d$ is the equivalent stiffness matrix and $\mathbf{p}^d$ is the equivalent nodal force vector.

Writing the matching conditions at the exposed surface, (5) and (6), in discretized form,

$$\mathbf{u}_{BC}^s = \mathbf{u}_{BC}^d = \mathbf{u}_{BC}, \tag{9}$$

$$\mathbf{p}_{BC}^s + \mathbf{p}_{BC}^d = \mathbf{q}. \tag{10}$$

A new global system of equations is formed by coupling the dielectric, equations (8), with the semiconductor, equations (7), and enforcing the matching conditions (9) and (10). vspace-0.1in

$$\begin{pmatrix} \mathbf{S}_{11} & \mathbf{S}_{12} & \mathbf{0} & \mathbf{0} \\ \mathbf{S}_{21} & \mathbf{S}_{22} & \mathbf{0} & \mathbf{I} \\ \mathbf{0} & \mathbf{K}_{12} & \mathbf{K}_{11} & \mathbf{0} \\ \mathbf{0} & \mathbf{K}_{22} & \mathbf{K}_{12}^T & -\mathbf{I} \end{pmatrix} \begin{pmatrix} \mathbf{u}_o^d \\ \mathbf{u}_{BC} \\ \mathbf{u}_o^s \\ \mathbf{p}_{BC}^s \end{pmatrix} = \begin{pmatrix} \mathbf{p}_o^d \\ \mathbf{q} \\ \mathbf{p}_f^s \\ \mathbf{0} \end{pmatrix}. \tag{11}$$

Solution of this set yields the potential distribution in the semiconductor domain, including the interface $\partial\Omega_{BC}$, and the nodal flux on $\partial\Omega_{BC}$.

IV. Example

The example structure with its dimensions is shown in Fig. 2. The quantum wire is realized at the $Al_{0.3}Ga_{0.7}As/GaAs$ heterojunction and is defined by the metal gates on the top surface. The gate electrodes have an applied voltage V_g. Between the gates is the exposed semiconductor surface where the interface charge density Q_{int} is assumed to be fixed for the example although this is not a limitation of the algorithm. The n-type doping density is assumed to be $10^{18}cm^{-3}$ in the $Al_{0.3}Ga_{0.7}As$ layer and $10^{15}cm^{-3}$ in the $GaAs$ substrate. A semi-classical Thomas-Fermi charge model [2, 7] is assumed in the semiconductor domain.

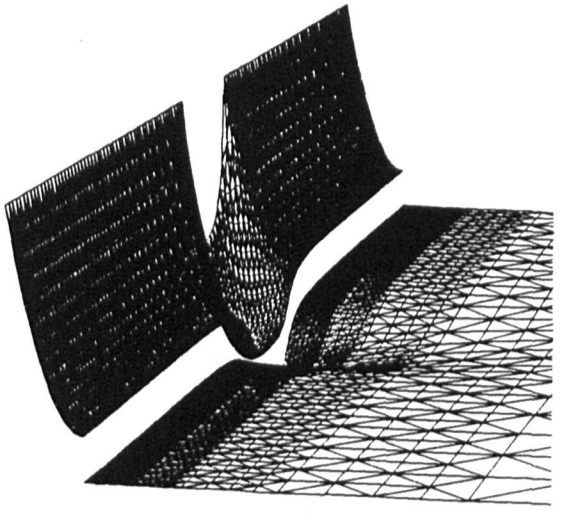

Figure 3: Sample result of the potential landscape in the semiconductor region. Shown is the conduction band obtained by the FBEM algorithm for -1.0V gate bias. The heterointerface is clearly visible at the discontinuity of the potential.

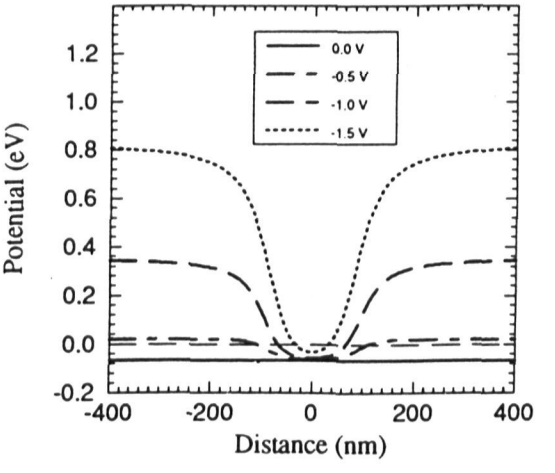

Figure 4: Result of the FBEM algorithm showing the conduction band profiles parallel to the heterointerface (on the GaAs side) for different bias conditions.

As shown in the center of Fig. 3, a potential well is formed underneath the exposed surface for a negative gate bias of -1.0 V. In Fig. 4, the conduction band is plotted parallel to the $AlGaAs/GaAs$ heterointerface (on the GaAs side) for different bias conditions. An electron gas is formed in those regions where the conduction band dips below the semi-classical electron quasi Fermi level, which is chosen as the zero of the energy axis and indicated by the dashed line. Figure 5 shows a comparison of the results obtained with our FBEM algorithm and those utilizing the conventional Dirichlet or Neumann boundary conditions. Shown is the conduction band profile parallel to the $AlGaAs/GaAs$ heterointerface (on the GaAs side) in Fig. 5(a), and the different methods produce significantly different results. Specifically, the expected width of the electron channel differs by a factor of two for the Dirichlet and FBEM boundary conditions. The Dirichlet boundary conditions also predict a significantly higher electron density than the FBEM algorithm. Figure 5(b) shows the same comparison at the semiconductor surface. Both the Dirichlet and Neumann boundary conditions exhibit an unrealistic discontinuous behavior of the potential, as opposed to the physically more appealing smooth result

of the FBEM algorithm.

In summery, we have presented a study of the boundary conditions at exposed semiconductor surfaces and developed an algorithm, termed FBEM, to solve this type of potential problem in the semiconductor and the dielectric. The major advantage of our algorithm is to model the exposed semiconductor surface by imposing the more physical interface matching conditions without making artificial assumption about either the potential or the electric field at the exposed surface. In ongoing work, we study the implementation of different physical models for the interface charge Q_{int} at the exposed surface. These results will be presented in the future.

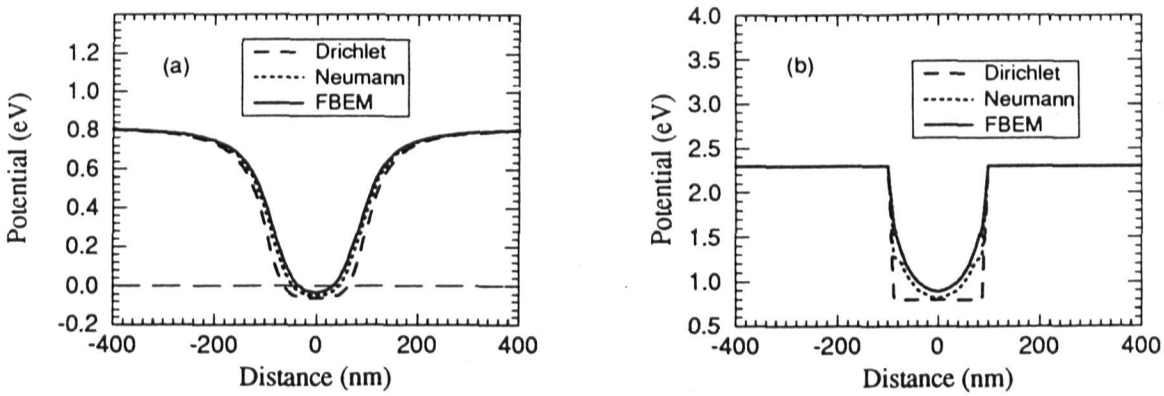

Figure 5: Comparison of the conduction band profiles under -1.5 V gate bias for the three types of boundary conditions on the exposed semiconductor surface; (a) parallel to the heterointerface (on the GaAs side), and (b) parallel to the semiconductor surface.

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