Optimization of Spin-Transfer Torque Magnetic Tunnel Junction-Based Logic Gates

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INTRODUCTION

By offering zero standby power, non-volatile logic is a promising solution to overcome the leakage losses which have become an important obstacle to scaling of CMOS technology [1]. Magnetic tunnel junctions (MTJs) offer a great potential, because of their unlimited endurance, CMOS compatibility, and fast switching speed. Recently, several realizations of MTJ-based logic gates have been demonstrated using spin-transfer torque (STT) MTJs for which the MTJ devices are used simultaneously as memory and logic gates [2], [3]. This intrinsically enables logic-in-memory architectures with no need for extra hardware [4]. The error probabilities in these gates depend significantly on device and circuit parameters. Here, we present a method to optimize the device and circuit parameters by minimizing the errors.

ERROR PROBABILITY CALCULATION

Fig. 1a and Fig. 1b show the STT-MTJ-based reprogrammable [2] and implication (IMP) [3] logic gates, respectively. Depending on the resistance (logic) states of the input (source) MTJ devices, these gates provide a conditional switching behavior on the output (target) MTJs. The error probability of the realized conditional switching behavior, which is corresponding to a specific Boolean logic operation, depends on the desired switching/non-switching event probabilities as

$$P_{\mathrm{err}} = \frac{1}{N}\sum_{i=1}^{N}\left\{\sum_{j=1}^{n_{\mathrm{u}}} P_{\mathrm{s}}(j) + \sum_{k=1}^{n_{\mathrm{d}}}[1 - P_{\mathrm{s}}(k)]\right\}, \quad (1)$$

where N is the total number of possible input states, n_{u} (n_{d}) is the number of undesired (desired) switching events, and P_{s} is the switching probability of the MTJ defined as [5]

$$P_{\mathrm{s}} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_{\mathrm{I}}\left(1 - \frac{I}{I_{\mathrm{C0}}}\right)\right]\right\}. \quad (2)$$

Δ_{I} is the thermal stability factor associated with the STT switching [6], t is the pulse width, and I is the current flowing through the MTJ. In order to calculate the current (I) passing through each MTJ the bias voltage dependence of the TMR ratio [5] must be taken into account [3].

RESULTS AND DISCUSSION

Fig. 2 shows P_{err} for different logic operations based on the reprogrammable gate as a function of V_{A}. It illustrates that for each operation there is an optimal V_{A} and the AND (NAND) operation demonstrates a lower error probability as compared to the OR (NOR) operation. Similar circuit parameter optimizations can be performed for IMP gate [3].

The minimum in total error probability is because of a trade-off between the probabilities of the desired and undesired switching events as shown in Fig. 3. As the state dependent modulation (SDM) increases with the tunnel magnetoresistance (TMR) ratio, the error probability decreases with the increase of the TMR (Fig. 4). Another important device parameter is Δ_{I} according to (2), higher Δ_{I} provides sharper switching dynamics, smaller SWs, and thus lower error probabilities (Fig. 5).

Note that a larger Δ_{I} is also needed for reliable operation of large STT-MRAM memory arrays [6]. From Fig.4 and Fig.5 we conclude that the implication logic architecture provides smaller error for probabilities logic operation and is thus preferred for logic-in-memory implementation.

ACKNOWLEDGMENT

The work is supported by the European Research Council through the grant #247056 MOSILSPIN.

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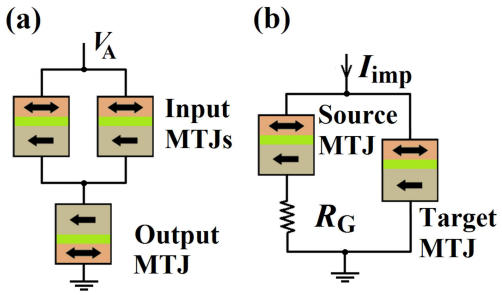

Fig. 1. (a) MTJ-based reprogrammable logic gate [2]. Depending on the preset state of the output MTJ and the polarity and amplitude of the applied voltage (V_A), the result of a logic operation (AND, OR, NAND, or NOR as shown in Fig. 2) between the inputs will be written in the output MTJ. (b) Current-controlled implication [3] logic gate. The resistance states of the target and source MTJs are the logical inputs and the final state of the target MTJ holds the output.

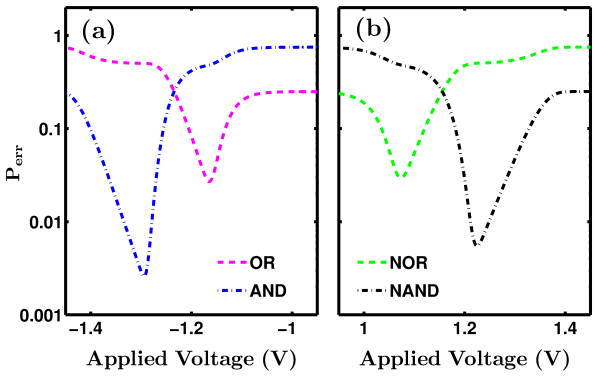

Fig. 2. Average error probabilities for different logic operations using the reprogrammable gate as a function of V_A based on physical MTJ devices characterized in [5]. The value of the circuit parameters (V_A in the reprogrammable gate and I_{imp} and R_G in the IMP gate) can be optimized to minimize the error probability (P_{err}).

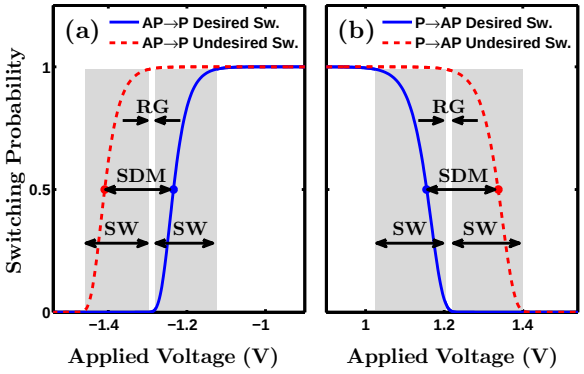

Fig. 3. Switching probabilities of the output MTJ (Fig. 1a) plotted for desired and undesired switching events in AND (a) and NAND (b) operations with the reprogrammable gate. A high enough state dependent modulation (SDM) can open a reliable gap (RG) between the switching windows (SWs).

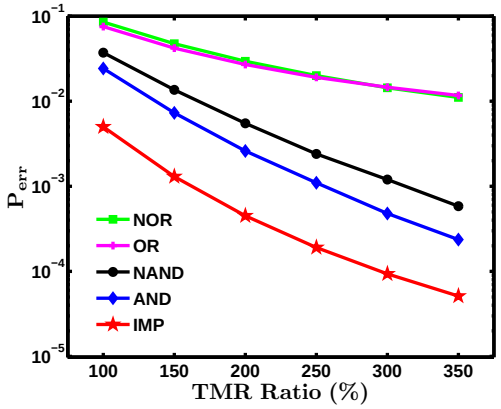

Fig. 4. Average error probabilities for implication and reprogrammable logic gates as a function of the TMR ratio plotted for optimized circuit parameters and $\Delta_I = 40$. Increasing the TMR ratio increases the SDMs shown in Fig. 3. Therefore, it increases RG and thus decreases P_{err}.

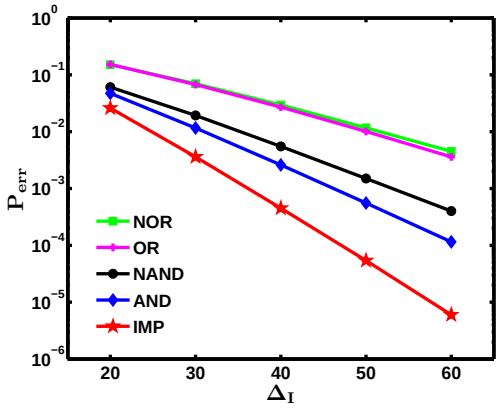

Fig. 5. Average error probabilities for implication and reprogrammable logic gates as a function of Δ_I plotted for optimized circuit parameters and TMR=200%. Increasing Δ_I decreases the SWs shown in Fig. 3 and therefore decreases P_{err}. The implication logic architecture significantly improves the reliability as compared to the reprogrammable logic architecture.