Study of the Role of Different Phonon Scattering Mechanisms on the Performance of a GAA Silicon Nanowire Transistor

M. Aldegunde, and A. Martinez

College of Engineering, Swansea University, Swansea SA2 8PP, United Kingdom e-mail: m.a.aldegunderodriguez@swansea.ac.uk

Abstract—In this paper we study the effect that different phonon scattering mechanisms have on the performance of a silicon gate-all-around nanowire field effect transistor (GAA NWFET). The study is carried out using the Nonequilibrium Green's function (NEGF) formalism in the effective mass approximation. We consider the impact of the bias conditions on the influence of the different phonons on the transport characteristics. We show a quantitative and qualitative difference in the behaviours of the impact of the different phonons for different bias conditions. The simulations including all phonons reproduce the correct behaviour of previous simulations using a sophisticated tight-binding/NEGF approach [1] while presenting a much lower computational effort suitable for technology computer aided design (TCAD) applications. Finally, we confirm that the addition of the phonon related resistivity from simulations including only selected phonons (as proposed in Matthiessen's rule) does not add up to the resistivity of the simulation including all phonons together, underestimating in this way the total phonon related resistivity by 13%.

I. Introduction

The Gate-All-Around Nanowire transistor (GAA NWT) architecture offers the best electrostatic integrity and therefore is a strong candidate to replace the traditional planar bulk MOSFETs for CMOS applications at the end of the road-map [2]. Their fabrication with a large variety of cross-sectional sizes and channel lengths has been previously demonstrated [3], [4]. Even though, at small channel lengths, electron transport was expected to be ballistic, it has been shown that for small NWT cross-sections the electron-phonon interaction increases and plays a major role in mobility degradation [5], [6], [7], [8], [9], [1], [10], [11]. Additionally, phonon scattering is the main source of de-coherence and energy relaxation in electron transport. Understanding the role of the different phonon mechanisms is important for TCAD applications in which accuracy as well as speed are paramount. Neglecting unimportant mechanisms can potentially save computational time. Previous works have carried out studies of the role of different phonons in nanowires [12], [13], explaining the physical effect of different types of phonons and analysing the impact of the value of different parameters which characterise the electron-phonon interaction. In this paper we focus on the impact of the different phonon scattering mechanisms

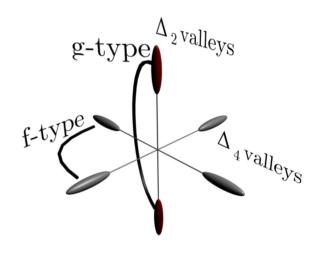


Fig. 1. Schematic of intervalley phonon-mediated transitions between the Δ valley minima in silicon. Δ_2 valleys are aligned with the axis of the nanowire, so that the confinement mass equals m_l in both directions.

in different working conditions of a Silicon GAA NWT using the Non-Equilibrium Green's Function (NEGF) formalism. The different biases induce different internal conditions. We explain how these influence the importance of the different types of phonons.

In Section II, we describe the simulation approach used to carry out this study. In Section III, we present the analysis of the impact on the drain current of the different phonons for different working conditions. Finally, the conclusions of this work are presented in Section IV.

II. SIMULATION APPROACH

The quantum carrier transport is described using the NEGF approach, using an effective-mass Hamiltonian. The effective masses were extracted from Tight Binding calculations to capture the dependence of the electron band structure on the nanowire diameter [14]. Since in this study we do not include any rough interface or discrete dopants, we use an uncoupled mode space approach, which allows for efficient calculations of nanowire transistors with gate lengths much longer than what would be possible using a full 3D approach.

Electron-phonon scattering has been included in the self-consistent Born approximation and using local self-energies. We have used phonon parameters extracted for bulk MOSFET structures widely used to reproduce the mobility of Si devices. Using these approximations, in a recent work [11] we showed a good agreement in the mobility and ballisticity of NWTs with simulations using more sophisticated models including the full phonon dispersion relations of the nanowire [1], [10].

Three types of f and g optical phonons are considered, which allow electron transitions between non-equivalent/equivalent valleys as shown in Fig. 1. Intravalley acoustic phonons are included in an elastic approximation. All phonon scattering parameters are the same as those used in [8], [11]. Using the mentioned approximations the self-energies for scattering with acoustic phonons can be written as:

$$\Sigma_v^{< n, n}(x_i; E) = |M_q|^2 \sum_m G_v^{< m, m}(x_i, x_i; E) F_{m, v}^{n, v}(x_i),$$

where n, m are sub-band indices, v the valley, x_i is the node in the longitudinal dimension, E is the energy, $|M_q|^2$ is the electron-phonon matrix element and F is the form factor,

$$F_{m,v}^{n,v'}(x_i) = \int dy \, dz \, |\psi_{x_i,v'}^n(y,z)|^2 |\psi_{x_i,v}^m(y,z)|^2. \quad (2)$$

For the optical phonons the self-energy is:

$$\Sigma_{j,v}^{< n,n}(x_i; E) = |M_q|^2 \left(N_j + \frac{1}{2} \pm \frac{1}{2} \right) \times \times \sum_{m,v'} g_j^{v,v'} G_{v'}^{< m,m}(x_i, x_i; E \pm \hbar \omega_j) F_{m,v'}^{n,v}(x_i),$$
(3)

where N_j is the average phonon occupation at the energy $\hbar\omega_j$ and $g_j^{v,v'}$ is a final valley degeneracy factor which equals $\delta_{v,v'}$ for g-type phonons and $2(1-\delta_{v,v'})$ for f-type phonons.

III. RESULTS

The simulation study was done using a silicon GAA nanowire transistor with a $2.2\times2.2~\text{nm}^2$ cross-section and 20 nm undoped channel. The equivalent oxide thickness of 0.8 nm. The source and drain extensions are 15 nm long with a uniform doping concentration of $10^{20}~\text{cm}^{-3}$. Fig. 2 shows the sub-band structure of this nanowire at low drain bias conditions. Fig. 3 shows the local density of states inside the device at the same bias conditions for the simulation including all the electron-phonons scattering mechanisms.

The transfer characteristics for the nanowire transistor are shown in Figs. 4 and 5 for drain biases of $V_D=1$ mV and $V_D=0.6$ V, respectively. The I_D-V_G for the ballistic transistor (B), the device with all phonon scatterings included (S), the device with only acoustic phonons included (A), the device with only g-type

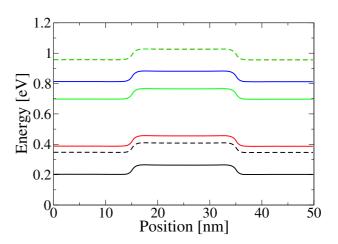


Fig. 2. Subband structure of the 20 nm gate length silicon nanowire transistor at $V_D=1$ mV and $V_G=0.7$ V. Continuous lines correspond to sub-bands of Δ_4 valleys (one confinement mass m_l and one m_t) and dashed lines to Δ_2 valleys (both confinements masses equal to m_l).

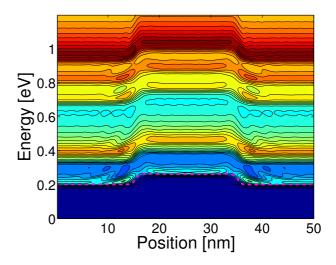


Fig. 3. Local density of states for the simulated device at $V_D=1\,$ mV and $V_G=0.7$ V. The lowest sub-band (magenta dashed line) is also plotted as a reference.

phonons (G), and the device with only f-type phonons (F) are shown. It is already clear from this figures that the f-type phonons have the lowest impact on the drain current of the transistor. On the other hand, the acoustic phonons produce the strongest reduction in current, especially in the sub-threshold regime.

This is analysed in more detail in Figs. 6 and 7, which show the drain current reduction defined as $(1 - I_{scat}/I_{ball})$ for both drain bias conditions. The results for the device (S) show a similar behaviour to that shown in [1], although the values of the reduction are slightly overestimated in our simulations. Acoustic phonon scattering is the main responsible for the reduction in the current at all bias conditions. This result is more pronounced at low drain bias conditions. However, the relative impact

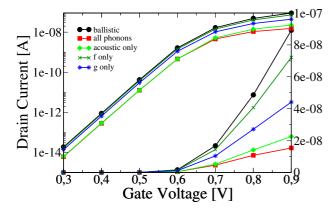


Fig. 4. The I_D-V_G characteristics at $V_D=1\,\mathrm{mV}$ for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

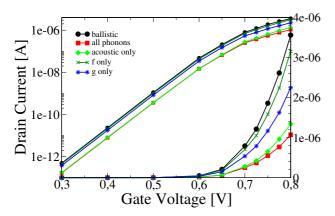


Fig. 5. The I_D-V_G characteristics at $V_D=0.6~\rm V$ for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

of this mechanism decreases with increasing gate bias, when the role of intervalley optical phonons becomes more important. There is, however, a clear difference, both qualitative and quantitative, in the dependence of the drain current reduction with the gate bias at low and high drain voltages. While at low drain voltage the impact of the acoustic phonon scattering keeps growing until $V_G = 0.9$, at high drain bias we can see a decrease of the drain current reduction for the (A) device starting at $V_G = 0.6$ V. For example, at $V_G = 0.9$ V and $V_D=1~\mathrm{mV}$ acoustic phonons produce a 75% lowering of the current, whereas at $V_D = 0.6$ V the drain current reduction for (A) drops to 50%. On the other hand, at low gate voltages the behaviour is similar in both situations (65%) and is dominated by acoustic phonon scattering. This change in the impact of acoustic phonon scattering makes the drain current reduction fall from 83% to 71% when the drain bias is increased from $V_D\,=\,1\,$ mV to $V_D = 0.6 \text{ V}$ if we include all phonons.

A. Matthiessen's rule

The extracted resistances at $V_D = 1$ mV and $V_G = 0.9$ V for (S), (A), (G) and (F) are 5.39×10^4 , 3.32×10^4 ,

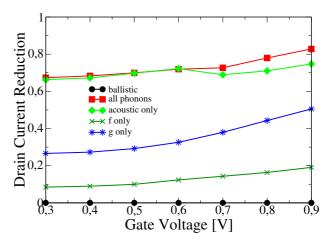


Fig. 6. Drain current reduction at $V_D=1\,\mathrm{mV}$ for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

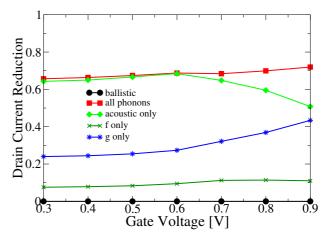


Fig. 7. Drain current reduction at $V_D=0.6~\rm V$ for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

 1.15×10^4 , and $2.7 \times 10^3~\Omega$, respectively. The resistance obtained from adding the devices (A), (G) and (F) is equal to $4.74 \times 10^4~\Omega$. This value is 12% lower than the value obtained for the device (S), which indicates that the Matthiessen's rule is violated in these nanoscale devices as already shown previously through semi-classical simulations [15], [16].

IV. CONCLUSION

We have studied the impact of different contributions to the electron-phonon scattering on the transfer characteristics of Si GAA NWFETs using the non-equilibrium Green's function formalism. We studied the impact of different bias condition on the drain current reduction induced by electron-phonon scattering. At low drain bias, the drain current reduction increases from 67% at low gate voltage to 83% in the on region. Most of the contribution comes from the acoustic phonon scattering, which produces a drain current reduction from 66% to

75% in the same range of gate biases when considered independently. Scattering by f- and g-type phonons are weaker. Their effect peaks at $V_G=0.9~\rm V$ and produce reductions of 19% and 50%, respectively. On the other hand, at high drain bias the gap between g-type and acoustic phonons is drastically reduced with the increase of gate bias beyond $V_G=0.6~\rm V$, when the difference in drain current reduction is only 7%. The trends for the drain current reduction when including all phonons are in a very good agreement with previously published results using more sophisticated transport models.

Finally, we studied the addition of the effect of the different phonons considered independently following Matthiessen's rule. We found a discrepancy of 13% between the phonon related resistivity in the simulation including all scattering mechanism and the addition of resistivities for individual simulations.

ACKNOWLEDGMENT

A.M. has been supported by an EPSRC Career Acceleration Fellowship, EP/I004084/1.

REFERENCES

- M. Luisier and G. Klimeck, "Atomistic full-band simulations of silicon nanowire transistors: Effects of electron-phonon scattering," *Phys. Rev. B*, vol. 80, no. 15, p. 155430, 2009.
- [2] H. Yan, H. S. Choe, S. Nam, Y. Hu, S. Das, J. F. Klemic, J. C. Ellenbogen, and C. M. Lieber, "Programmable nanowire circuits for nanoprocessors." *Nature*, vol. 470, no. 7333, pp. 240–4, Feb. 2011.
- [3] T. Y. Liow, K. M. Tan, R. T. P. Lee, M. Zhu, B. L.-H. Tan, G. S. Samudra, N. Balasubramanian, and Y. C. Yeo, "5 nm gate length Nanowire-FETs and planar UTB-FETs with pure germanium source/drain stressors and laser-free Melt-Enhanced Dopant (MeltED) diffusion and activation technique," in 2008 Symposium on VLSI Technology. IEEE, Jun. 2008, pp. 36–37.
- [4] S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Yeo, K. H. Cho, I. K. Ku, H. Cho, W. Jang, D.-W. Kim, D. Park, and W.-S. Lee, "Investigation of nanowire size dependency on TSNWFET," in 2007 IEEE International Electron Devices Meeting. IEEE, Dec. 2007, pp. 891–894.
- [5] S. Poli and M. G. Pala, "Channel-Length Dependence of Low-Field Mobility in Silicon-Nanowire FETs," *IEEE Electron Device Lett.*, vol. 30, no. 11, pp. 1212–1214, 2009.

- [6] K. Rogdakis, S. Poli, E. Bano, K. Zekentes, and M. G. Pala, "Phonon- and surface-roughness-limited mobility of gate-allaround 3C-SiC and Si nanowire FETs." *Nanotechnology*, vol. 20, no. 29, p. 295202, 2009.
- [7] M. Lenzi, P. Palestri, E. Gnani, S. Reggiani, A. Gnudi, D. Esseni, L. Selmi, and G. Baccarani, "Investigation of the Transport Properties of Silicon Nanowires Using Deterministic and Monte Carlo Approaches to the Solution of the Boltzmann Transport Equation," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2086–2096, 2008.
- [8] S. Jin, M. V. Fischetti, and T.-w. Tang, "Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity," J. Appl. Phys., vol. 102, no. 8, p. 083715, 2007.
- [9] S. Jin, Y. J. Park, and H. S. Min, "A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions," *J. Appl. Phys.*, vol. 99, no. 12, p. 123719, 2006.
- [10] M. Luisier, "Phonon-limited and effective low-field mobility in n- and p-type [100]-, [110]-, and [111]-oriented Si nanowire transistors," *Applied Physics Letters*, vol. 98, no. 3, p. 032111, 2011.
- [11] M. Aldegunde, A. Martinez, and A. Asenov, "Non-equilibrium Greens function analysis of cross section and channel length dependence of phonon scattering and its impact on the performance of Si nanowire field effect transistors," *J. Appl. Phys.*, vol. 110, no. 9, p. 094518, 2011.
- [12] N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, P. Razavi, R. Yu, G. Fagas, and J.-P. Colinge, "Effect of intravalley acoustic phonon scattering on quantum transport in multigate silicon nanowire metal-oxide-semiconductor field-effect transistors," J. Appl. Phys., vol. 108, no. 3, p. 034510, 2010.
- [13] N. D. Akhavan, A. Afzalian, A. Kranti, I. Ferain, C.-W. Lee, R. Yan, P. Razavi, R. Yu, and J.-P. Colinge, "Influence of Elastic and Inelastic ElectronPhonon Interaction on Quantum Transport in Multigate Silicon Nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1029–1037, Apr. 2011.
- [14] A. Martinez, M. Bescond, J. R. Barker, A. Svizhenko, M. Anantram, C. Millar, and A. Asenov, "A Self-Consistent Full 3-D Real-Space NEGF Simulator for Studying Nonperturbative Effects in Nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2213–2222, 2007.
- [15] A. K. Saxena and M. A. L. Mudares, "Validity of Matthiessens rule for calculating electron mobility in Ga1xAlxAs alloys," J. Appl. Phys., vol. 58, no. 7, p. 2795, 1985.
- [16] D. Esseni and F. Driussi, "A Quantitative Error Analysis of the Mobility Extraction According to the Matthiessen Rule in Advanced MOS Transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2415–2422, 2011.