

NBTI Product Level Reliability Challenges

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INTRODUCTION

The gate dielectric has been the subject of constant improvement and innovation since the invention of the MOSFET transistor. The gate oxide is the major transistor component to control the transistor channel underneath with respect to leakage currents as well as saturation drive currents. The demand for higher drive currents and better performance has also pushed the gate oxide thickness towards its material limits, especially as we enter the 65nm technology node. The common candidate for the ultimate gate dielectric, silicon dioxide, is facing its structural boundaries and silicon dioxide/nitride stacks will become main stream for 65nm technologies and beyond. Since the introduction of heavily nitrated gate oxides the NBTI phenomena gained significantly on importance. Extensive work has been published on the NBTI reliability for standard DC test conditions ($V_s, V_d, V_b=0.0V$) as well as under pulsed conditions. However, the role of hydrogen is still not fully understood [1]. Less work was published on the circuit level reliability degradation due to NBTI and the impact of relaxation. This work is analyzing all possible circuit level biasing conditions, maximum operating temperatures, and operating cycles to understand the impact on the circuit level. A simple analytical reliability model is referenced to estimate the threshold voltage shift during real operation conditions. This additional threshold voltage shift is counting against the design margin budget and, hence, has to be added to the SS corner at elevated temperature in order to evaluate the worst case circuit conditions.

TRANSISTOR LEVEL RELIABILITY

Numerous transistor level reliability data and degradation curves have been published in the recent literature on NBTI. A typical threshold degradation plot for a 90nm PMOS transistor is shown in Fig.1. The same gate oxide measured in a package level testing system which has a relaxation between the stress and the measurement cycle of 700ms is shown in Fig.2. It can be clearly shown that relaxation gives false readings in the early phases of the stress experiment, whereas the

degradation curves converge at higher stress levels suggesting that recovery is limited at longer stress intervals. The recovery phenomenon has been reported extensively in the literature and was attributed to the re-passivation of the broken Si-H bonds at the Si-Gate oxide interface by molecular hydrogen [2]. Almost 40% of the damage recovers after 30min of relaxation (see Fig.3). Whether to achieve higher level of recovery depends on the local stress equilibrium at the gate oxide and the availability of hydrogen to passivate the Si-H bonds. Fig.4 gives a PMOS transistor which has been stressed up to a certain stress time at a constant bias and afterwards different stress bias conditions have been applied. It is worth noting that the new equilibrium established fairly quickly and in the case of a lower stress voltage a recovery of NBTI degradation occurred for the 1.35V stress condition. Recently, it has been shown that NBTI lifetime under low frequency stress can be enhanced by a factor of 10 as compared to the DC NBTI lifetime [3,4]. Similar results are given in Fig.5 and a comparison with simulation results using a reaction based diffusion model to predict the DC and AC degradation [5] is given.

PRODUCT LEVEL RELIABILITY

Fig.6 shows the product level NBTI stress data for a low power asynchronous SRAM memory. We selected the access time as quality criterion to evaluate the NBTI lifetime. The memory is stressed at constant accelerated DC bias and temperature and different read points are acquired for the access time T_{aa} at 0.5, 1, 2, 3 and 4hours. The T_{aa} push out caused by NBTI stress is then used to extract the lifetime using a power law dependence. T_{aa} reflects well the NBTI related degradation behavior. The lifetime slope was correlated to single transistor data and showed good agreement.

CONCLUSION

Transistor and product level reliability data have been presented and correlated. It is important to notice that product level reliability is at least an order of magnitude higher compared to the transistor level reliability lifetime.

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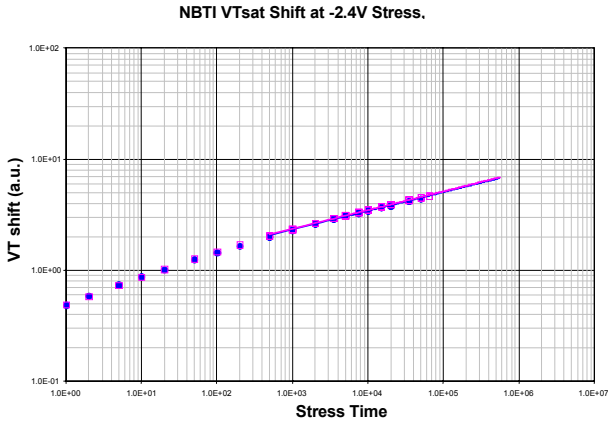


Fig. 1. Stress plot for extrapolation of NBTI lifetime for a 10/10 90nm PMOSFET device. The lifetime can be extrapolated for different Vtsat criteria.

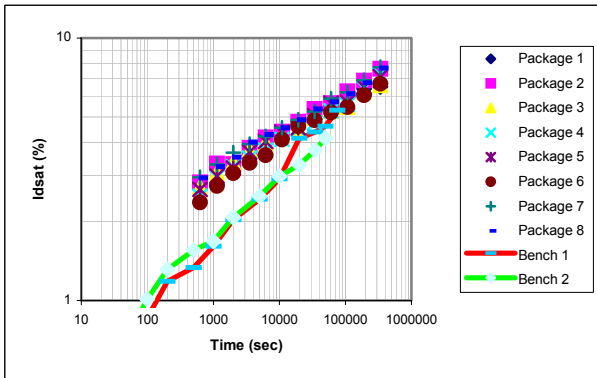


Fig. 2. NBTI Idsat degradation for different S-M-S methods. Package level (Symbols) and bench (lines) testing show the impact of relaxation at the early stress phases.

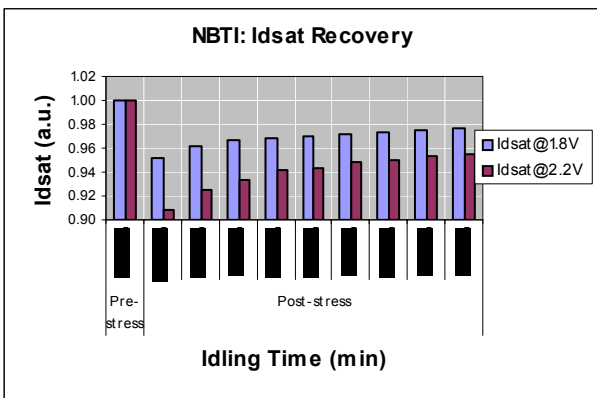


Fig. 3. Idsat recovery vs. relaxation time for 90nm PMOSFET. Almost 40% of the degradation recovers after 30min.

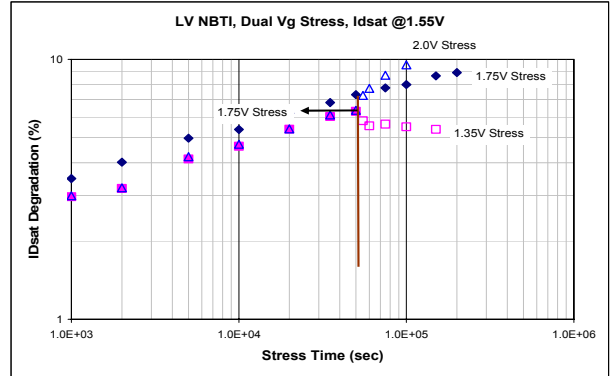


Fig. 4. NBTI degradation dependence on local stress equilibrium. Recovery can be found for switching to lower stress voltages.

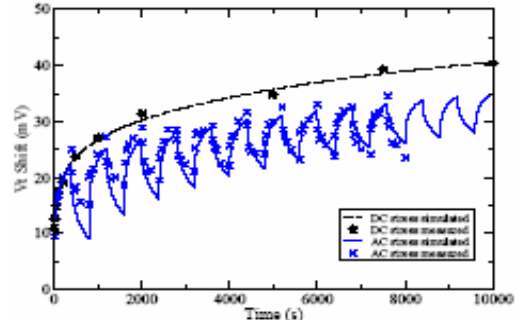


Fig. 5. NBTI degradation for a DC vs. 200kHz AC signal. Significant improvement is found for AC stressing.

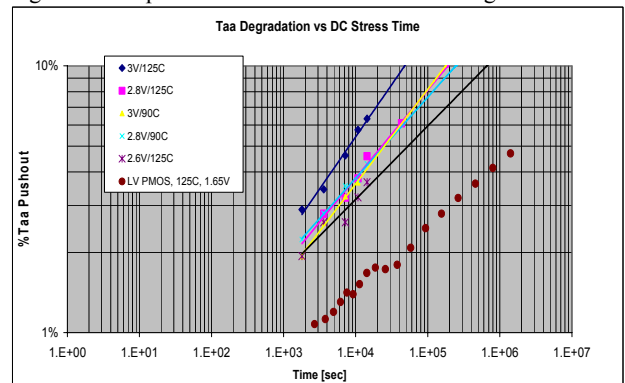


Fig. 6. Asyn SRAM memory Taa pushout due to NBTI stress for different temperatures and stress voltages .

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