Self-Consistent Treatment of Quantum Transport in 10-nm FinFET Devices Using CBR Method

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In order to investigate quantum transport properties in open 3D systems in sub-nanometer regime, a highly efficient numerical approach is essential. We have utilized the Contact Block Reduction (CBR) method [1-3] to simulate a variety of nano-scale FinFET devices self-consistently.

In this work the band-structure has been modeled by a single parabolic band with anisotropic effective mass for silicon and a spherical mass for the oxide. The exchange-correlation potential has been taken into account via the local density approximation. Real-space treatment of surface roughness and the effect of scattering (via a simple phenomenological model) have also been included. The self-consistent potential and current are obtained as converged solutions of the open-system Schrödinger equation coupled with the Poisson equation. This is achieved by employing the CBR method based on the Green's functions formalism, and a predictor-corrector approach, which has been modified for a superior convergence rate for open quantum systems. In the latest version of our CBR code, the appropriate number of eigenstates and lead modes used in the calculation is determined dynamically for each iteration, which helps to further reduce the computational time and makes it easier to simulate devices of arbitrary structure and with any number of leads.

Several FinFET devices shown in Fig. 1 with varying fin width have been simulated. Gate lengths of 10 nm and oxide thickness of 1.75 nm have been used in all the simulations. The fin is assumed to be lightly doped with a thickness varying from 6 nm to 12 nm. For the 12 nm fin width our simulation shows the formation of a distinct channel on each side of the fin (Fig. 2, left panel). As fin width decreases gradually from 12 nm towards 8 nm, inversion layer formed adjacent to both gates merge into a single channel as shown in Fig. 2 (middle and right panel).

The transfer characteristics for different fin widths are shown in Fig. 3, left panel. The data for 12nm fin width near subthreshold regime is in good correspondence to the experimental data [4]. We found that the effect of the fin width variation is more important for the subthreshold device behavior than for higher gate voltages (the linear scale is not shown here).

The device turn-off behavior has been examined by extracting sub-threshold slope for different fin widths. The corresponding data are shown on Fig. 3, right panel. It has been found that as the fin width decreases, the gate control improves *linearly* up to the fin width of 8 nm and then saturates with the further decreasing of the fin width. For 12 nm fin width the calculated value of the subthreshold slope is 126 mV/dec, as compared to 125mV/dec experimental value in Ref. [4].

The fully quantum mechanical approach utilized in the CBR method enables one to calculate the gate leakage with no additional computational costs, which might be impossible or difficult using other approaches. While the precise values of the gate currents are naturally very sensitive to the oxide thickness and the quality of Si/SiO_2 interface (simulated using an adjustable surface roughness parameter in the code), the trend of the simulated gate current matches closely the experimental data.

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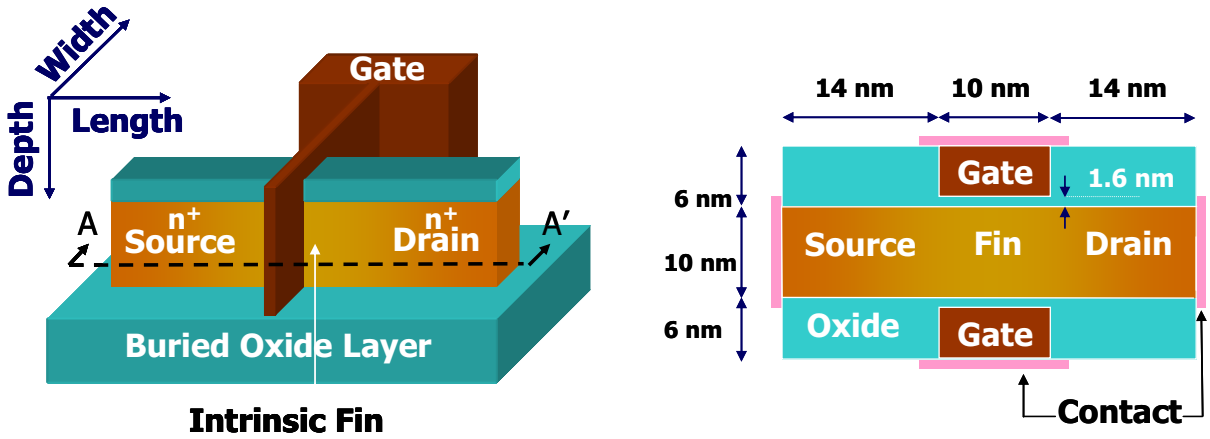

Figure 1. Left panel – 3D schematic view. Right panel – top view along A-A' cross section.

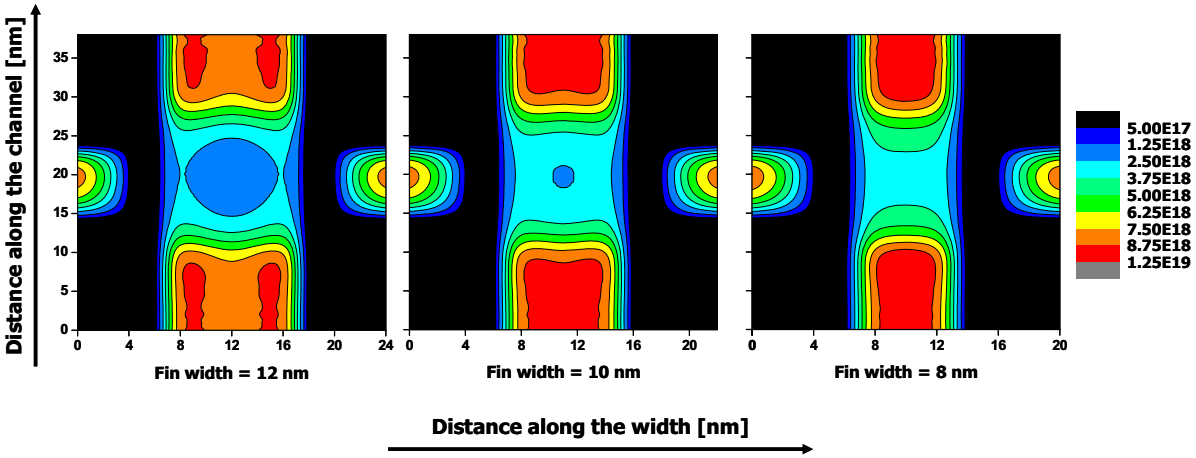

Figure 2. Electron density along A-A' cross section. Left panel: fin width=12nm, middle panel: fin width=10nm, right panel: fin width=8nm.

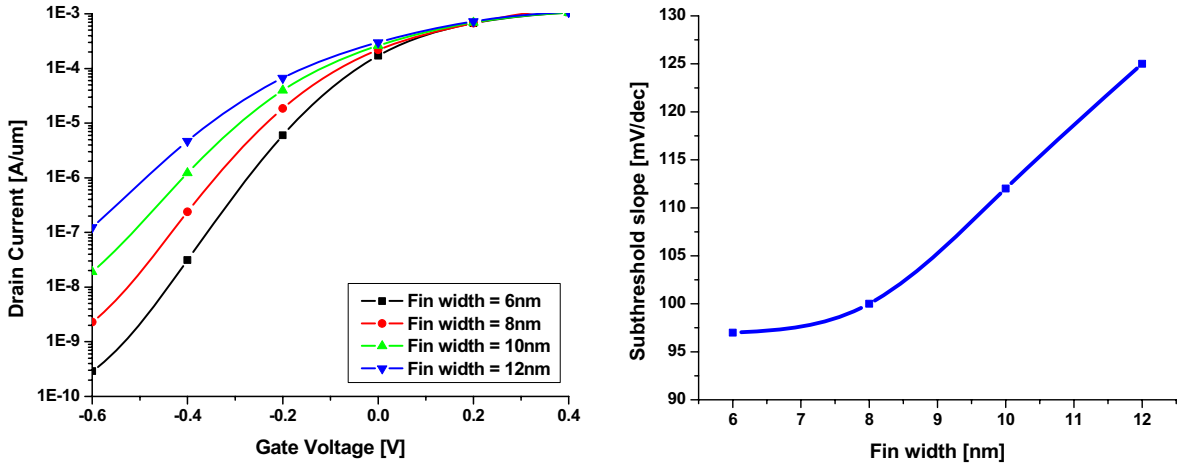

Figure 3. Left panel - transfer characteristics, $V_D = 0.1V$. Right panel – subthreshold slope vs. fin width.