11th International Workshop on Computational Electronics
TU Wien, 25-27 May 2006

A 3D Parallel Simulation of the Effect of Interface Charge Fluctuations in HEMTs

N. Seoane*, A. J. Garc´a-Loureiro*, K. Kalna†, and A. Asenov†
*Department of Electronics and Computer Engineering, Univ. Santiago de Compostela
15782 Santiago de Compostela, Spain. E-mail: natalia@dec.usc.es
†Device Modelling Group, Dept. Electronics & Electrical Engineering, University of Glasgow
G12 8LT Glasgow, United Kingdom

A 3D parallel device simulator is employed to study the impact of charge uctuations in the recess region of nanometre scale HEMTs. The simulator [1] is based on a drift-diffusion (D-D) approach using nite element discretisation on an unstructured tetrahedral mesh [2]. In order to reduce computational time, the simulator is parallelised via the MPI library. Fig. 1 shows the parallel ef cienc y obtained using the 3D D-D device simulator for the solution of Poisson's equation at equilibrium using a mesh with 76500 nodes.

The intrinsic parameter uctuations are expected to affect the RF performance and the matching of submicron HEMTs [3]. Random variations in the Si δ-doping and In content of the channel ternary alloy will induce significant parameter uctuations in I_D-V_G characteristics of 50 nm gate length InP HEMTs [3]. In this work we study the effect of interface charge uctuations in the recess regions of HEMTs on device characteristics and compare it with the effect induced by charge uctuations in the δ-doping layer and by variations in the ternary alloy content. Fig. 2 shows the difference between the electron densities at equilibrium for a 120 nm pseudomorphic HEMT (PHEMT) with and without interface charge. The electron density is plotted along a plane in the middle of the channel. We have assumed uniformly distributed interfacial charge of $-2 \times 10^{12}\text{cm}^{-2}$ at the recess region surface.

The effect of the interface charge is studied in two different HEMTs: (i) a 120 nm gate length PHEMT with an $In_{0.2}Ga_{0.8}As$ channel on GaAs substrate and (ii) a 50 nm gate length InP HEMT with an $In_{0.7}Ga_{0.3}As$ channel. The I_D-V_G characteristics of the transistors have been calibrated at low and high drain biases. The calibration was carried out in comparison with the measured data obtained from real devices fabricated at Glasgow and with data obtained from Monte Carlo (MC) device simulations [4, 5]. Note that the external resistances associated with the contacts have to be included in simulated I-V characteristics [6] for a fair comparison with measured data. Figs. 3 and 4 compare simulated and measured I_D-V_G characteristics for the 120 nm PHEMT at drain biases of 0.1 and 1.0 V respectively. The results obtained from the 3D parallel D-D simulator with the presence of interface charge in the recess regions (at the source and drain sides of the device) are also shown. The results of the MC simulations, which have only been carried out without interface charge, are presented for comparison. The interface charge lowers the drive current and the lowering increases at $V_D = 1.0$ V. Similar calibration and simulations are carried out for the 50 nm InP HEMT. Figs. 5 and 6 compare I_D-V_G characteristics at drain biases of 0.1 and 0.8 V respectively, for the 50 nm transistor. The effect of interface charge is smaller compared to the effect in the 120 nm PHEMT but the qualitative behaviour is similar. A statistical study of the effect of uctuations in the discrete interface charge in the recess regions on the characteristics of both HEMTs will be reported at the conference.

REFERENCES

[1] A. J. Garc´a-Loureiro, K. Kalna and A. Asenov, *Efficient three-dimensional parallel simulations of PHEMTs*, Int. J. Numer. Model.-Electron. Netw. Device Fields **18**, 327-340 (2005).

[2] P. A. Markowich, *The stationary semiconductor device equations*, Computational Microelectronics, Springer-Verlag (1986).

[3] N. Seoane, A. J. Garc´a-Loureiro, K. Kalna and A. Asenov, *Discrete doping fluctuations in the delta layer of a 50 nm InP HEMT*, in Proc. Workshop on Modeling and Simulation of Electron Devices, ed. by A. Campera, G. Fiori, G. Iannaccone, and M. Macucci, (Pisa, Italy, 2005) 78-79.

[4] K. Kalna, S. Roy, A. Asenov, K. Elgaid and I. Thayne, *Scaling of pseudomorphic high electron mobility transistors to decanano dimensions*, Solid-State Electron. **46**, 631-638 (2002).

[5] K. Kalna, K. Elgaid, I. Thayne and A. Asenov, *Modelling of InP HEMTs with high Indium content channels*, Proc. Indium Phosphide and Related Materials, 61-65 (2005)

[6] S. Babiker, A. Asenov, N. Cameron and S. P. Beaumont, *A simple approach to include external resistances in the Monte Carlo simulation of MESFETs and HEMTs*, IEEE Trans. Electron Devices **43**, 2032-2034 (1996).

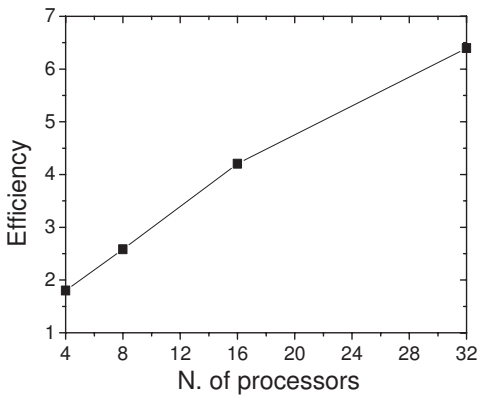

Fig. 1. Parallel ef cienc y for the solution of Poisson's equation at equilibrium using a 76500 node mesh.

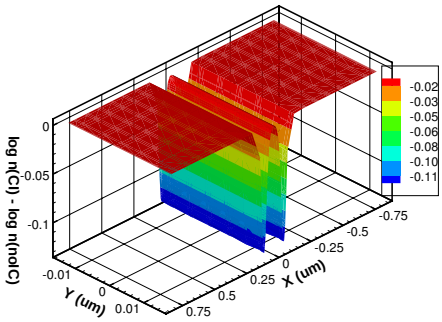

Fig. 2. Difference in electron density at equilibrium between a device with an interface charge of $-2 \times 10^{12} \mathrm{cm}^{-2}$ in the recess layer and a device without the interface charge, in a plane along the 120 nm PHEMT InGaAs channel. The x-axis is along the device with the zero set in the middle of the gate and the y-axis is along the device width.

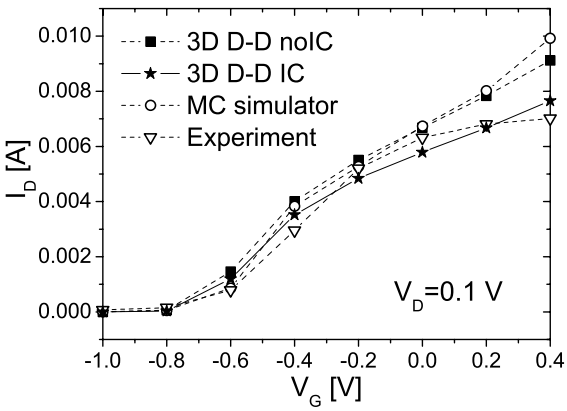

Fig. 3. I_D-V_G characteristics at V_D=0.1 V for the 120 nm PHEMT. Full squares are for 3D D-D simulations with excluded interface charge and stars are for 3D D-D simulations with included interface charge. All simulations, including MC results, represent an intrinsic device. Experimental data are also shown for a comparison.

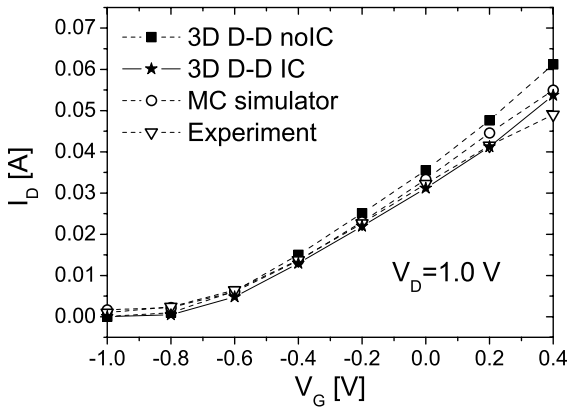

Fig. 4. I_D-V_G characteristics at V_D=1.0 V for the 120 nm PHEMT. The symbols have the same meaning as in Fig. 3.

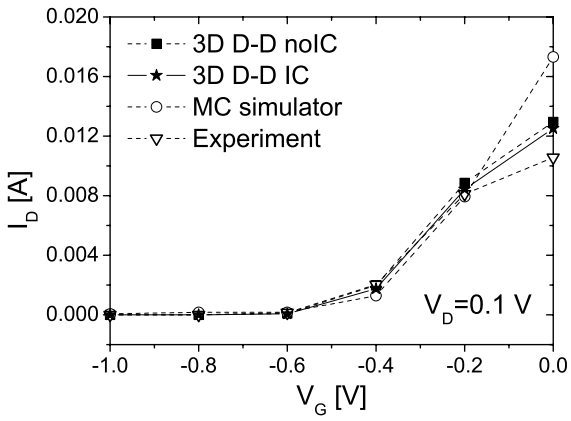

Fig. 5. I_D-V_G characteristics at a low drain bias of 0.1 V for the 50 nm InP HEMT. The results obtained from the 3D D-D simulator with interface charge excluded (full squares) and included (stars), and MC results are shown, all for an intrinsic device. Experimental data given by open triangles are presented for a comparison.

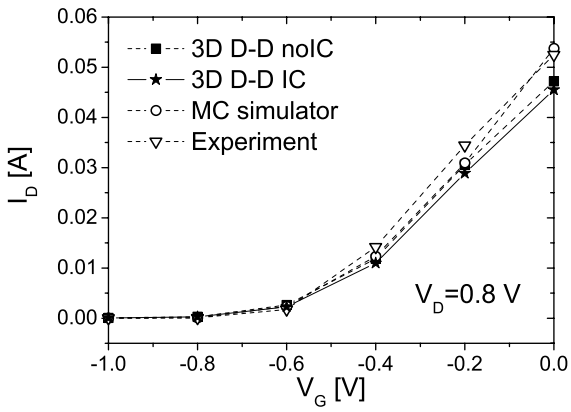

Fig. 6. I_D-V_G characteristics for the 50 nm InP HEMT. The same data from 3D D-D and MC device simulators as in Fig. 5 are shown but at a high drain voltage of 0.8 V.