11th International Workshop on Computational Electronics
TU Wien, 25-27 May 2006

Semiconductor Transport Modeling for the Analysis of Nanoscaled CMOS Circuits

F. Felgenhauer, M. Begoin, J.-K. Bremer, and W. Mathis
Institute for Theoretical Electrical Engineering, Uni Hannover, Appelstr., 9A Hannover, Germany
e-mail: felgenhauer@tet.uni-hannover.de

***Abstract*— We discuss the influence of quantum effects in highly scaled CMOS circuits. On the base of 1-d numerical simulations for transport in mesoscopic systems, we set up Spice circuit models. With this Spice models rebuilding the influence of quantum effects, the functionality of classical circuit concepts can be 'tested' in their robustness against these effects. A few circuit examples will be given.**

DISCUSSION

The most important quantum effects for MOS devices in the sub 100nm regime are direct tunneling currents (edge-direct and channel-direct tunneling), charge quantization in the inverted channel and quasi-ballistic transport in very short channel devices. All these effects are pure parasitics influencing or significantly disturbing the device performance. Since CMOS is dominating the semiconductor industry it is very important to ensure that conventional circuit concepts are still applicable when the devices are scaled into the sub 100nm regime. Instead of developing complete new device models we restrict ourselves on the quantum-mechanical description of transport problems, which cause parasitic noise in MOS devices and analyse CMOS circuits under the direct influence of quantum effects. The quantum transport is described in terms of the Schrödinger equation with spatial dependent mass

$$\left[-\frac{\hbar^2}{2}\frac{d}{dx}\frac{1}{m^*(x)}\frac{d}{dx}+v_{\text{eff}}(\mathbf{k}_t,x)\right]\psi(x)=\varepsilon_x^L\psi(x) \tag{1}$$

with

$$v_{\text{eff}}(\mathbf{k}_t,x)=v_{\text{coul}}(x)+E_c(x)+\frac{\hbar^2k_t^2}{2m_L^*}\left(1-\frac{m_L^*}{m^*(x)}\right).$$

With the restriction to pure Coulomb interaction, the solution of (1) is coupled with the Poisson equation

$$\frac{d}{dx}\epsilon(x)\frac{d}{dx}v_{\text{coul}}(x)=-q^2[n(x)-N_D^+(x)+N_A^-(x)] \tag{2}$$

according to the Hartree approximation. For more details please see [1]. We implemented a 1-d numerical self-consistent solver (see figure 1,2,3), whereby we use the NEGF formalism for the Schrödinger equation and the Newton-Raphson method for the Poisson equation. The primary goal we want to achieve with the quantum transport calculation is the estimation of tunneling currents for circuit applications, as we already emphasized in the beginning. The advantage of the use of the NEGF formalism, is that it intrinsically enables the inclusion of more sophisticated interactions in devices. Thus we are able to calculated more parasitic quantum effects, which is our future goal.
Using the numerical simulations we build Spice circuit models to include influence in circuit simulations. One example to show a functionality breakdown in a dynamic logic circuit caused by tunneling currents is the Domino-AND-2-gate (suggested by Choi et al. [2]). We simulated this circuit (see figure 4) using a corresponding Spice model for edge-direct tunneling in transistor M2. For the input signal sequence shown in figure 5 the circuit is producing two logic errors at the output (figure 6).

REFERENCES

[1] F. Felgenhauer Maik Begoin and Wolfgang Mathis. *Transistor Level Modeling for Analog/RF IC Design*, chapter On Incorporating Parasitic Quantum Effects in Classical Circuit Simulations. Springer Verlag, to be published in 2006.

[2] Choi CH, Nam KY, Yu Z, Dutton RW. Impact of gate direct tunneling current on circuit performance: a simulation study. *IEEE Transactions on Electron Devices* 2001; **48**(12):2823–2829.

ISBN 3-901578-16-1

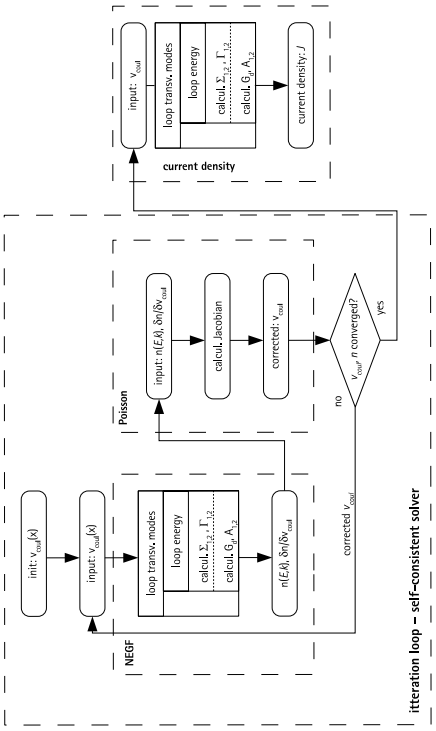

Fig. 1. Flowchart self-consistent solution

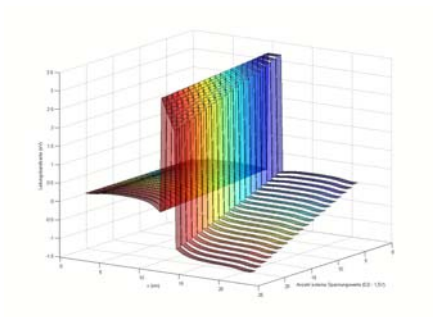

Fig. 2. Potential profile for 1.8nm SiO_2 barrier

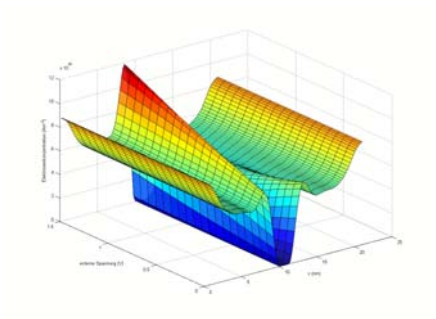

Fig. 3. Charge concentration profile for 1.8nm SiO_2 barrier

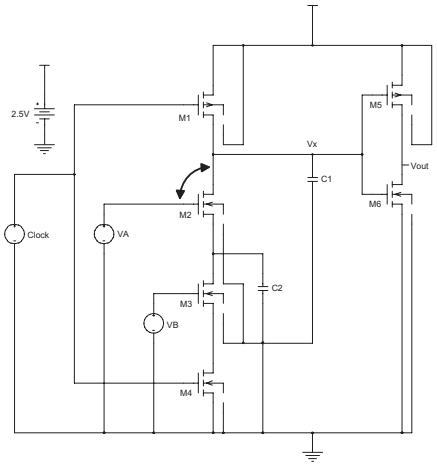

Fig. 4. Domino AND 2 Gate

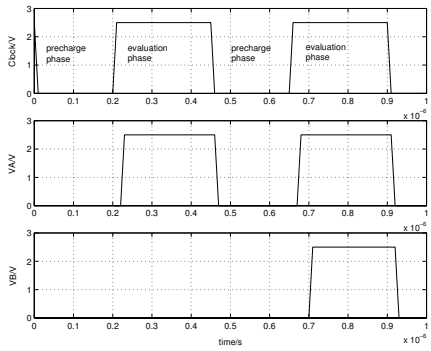

Fig. 5. Input signals for Domino AND 2 Gate

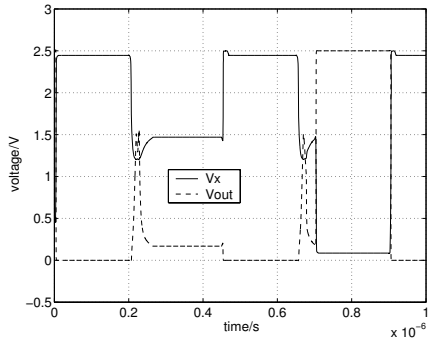

Fig. 6. Output signals for Domino AND 2 Gate