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Combined Line-Width-Roughness (LWR) and Local Critical Dimension (CD) Variation Effects on Sub-65nm MOSFET Current – Voltage Characteristics: From Lithography to Metrology to Device Simulation

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INTRODUCTION

Various characterization methods and lithography technologies using new resist materials and advanced gate patterning processes to reduce line-edge roughness (LER) have been developed, but the aggressively continuing progress in CMOS technology calls for more detailed understanding, quantification and estimation of LER/LWR effects on the electrical behavior of future scaled MOS transistors. Simple statistical analysis has shown that the gate patterns without the appropriate LWR control may cause severe fluctuations in device parameters and performance, especially in the nanometer scaled MOSFET technologies, resulting in a negative average threshold voltage shift, a sub-threshold slope degradation, an unrealistic effective channel length extraction and an exponential increase in off-state leakage current [1],[2].

Our metrological work has shown that LWR is not a value but a function of the width of the transistor [4]. LWR increases with transistor width and saturates at large ("infinite") widths on the order of 2μm. For smaller widths LWR is not independent but it is coupled to local CD variation. LWR is reduced at small widths while CD variation increases keeping the sum of their squares constant (this value is termed sigma "infinite"). The interplay between LWR and CD variation depends on the LWR spectrum, i.e. the correlation length ξ and the roughness exponent α (related to the fractal dimension of the transistor edges). Thus LWR is a function described with three parameters namely "sigma infinite", correlation length ξ, and roughness exponent α.

WORK DESCRIPTION

This work has two goals: First, using simple analytic models to examine the effect of combined LWR and CD variation on transistor operation, and the relevant importance of each effect. In addition we explore how the transistor operation is influenced by the triad of the LWR parameters, hence from the whole LWR spectrum. This part of our work connects LWR metrology to device operation. In order to evaluate LWR effects on device current behavior we follow an analogous approach as is described in [2].

Specifically, the total gate width W is divided into N segments with no LWR and with a certain characteristic width ΔW=1-5nm (Fig. 1). The drain current of the whole gate is calculated by summing the N gate segments in parallel. The drain current of each segment is given by simple or more complicated analytical formulas including short channel and narrow width effects. By the drain current vs. gate voltage curve, the threshold voltage shift of the total gate can be estimated. The calculation is repeated for a large number of gates with specific LWR parameters so that sufficient statistics is obtained. First results for the dependence of these shifts on the spatial LWR parameters (α,ξ) are shown in Fig.2. The standard deviation of these values as well as the off-current for the whole spectrum of (α,ξ) will be also presented in the work. Furthermore, the effects of

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the gate width W and length on these dependencies will be also examined.

Second we connect the lithography process and material architecture to the device operation. Here, LWR is introduced through the explicit stochastic simulation of the processes leading to the development of photoresist lines (Fig.3), and assuming that LWR introduced in the final transistor gate will be a modulation of this initial photopolymer LWR, after silicon etching, doping, and annealing [3]. Then LWR effects on device operation are evaluated as above (Fig. 1), where ΔW now indicates the photopolymer chain monomer size. The result of this second part of our work is to connect the LWR effects on the device to photoresist molecular weight and polymer chain architecture, for both conventional and chemically amplified photopolymers. The effects of transistor width will be also investigated.

ACKNOWLEDGEMENT

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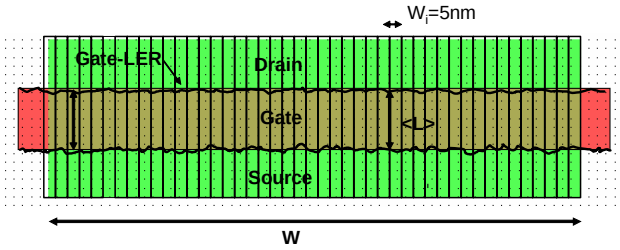

Fig. 1. The transistor is divided into sub-transistors.

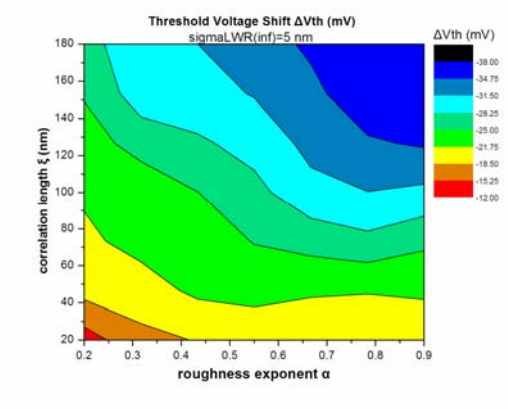

Fig. 2. Effect of correlation length and roughness exponent on threshold voltage shift for W=135nm, ΔW=5nm and CD nominal=45nm.

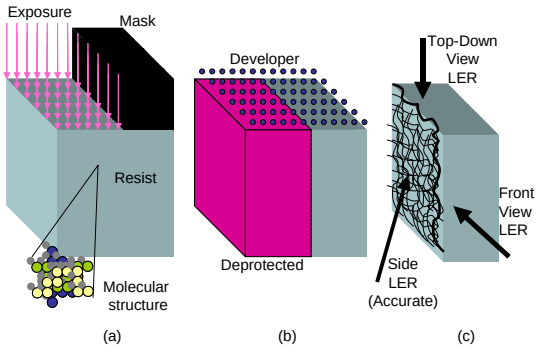

Fig. 3. Qualitative picture of process simulation. (a) Material placement in lattice, and exposure. (b). Acid-diffusion simulation and creation of deprotection sites. Beginning of development. (c). Measurement of edge roughness.