11th International Workshop on Computational Electronics
TU Wien, 25-27 May 2006

Calculating Future CMOS and CMOS Future - - Where Industry Needs Academia

T. Skotnicki & H. Jaouen
STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France
e-mail: thomas.skotnicki@st.com

INTRODUCTION

During the last 30 years the number of transistors per chip has increased X100 000, that is even more (10 times) than the predictions of Moore's laws, see Fig. 1. The transistor has decreased X320, bringing its feature dimensions close to the atomic resolution scale, see Fig. 2. Consequently, the now-a-day circuits present a tremendous complexity of NANO-objects, in the order of 1e9 per chip. All of those objects (mainly transistors) are governed to large extend by quantum solid-state physics. Their fabrication to be controlled also requires the more and more sophisticated models and tools. In this paper we will review the main issues and needs the IC industry encounters with this respect.

FUTURE CMOS

The time constant for introduction of new technologies in CMOS industry may go up to 10 years, especially if development of specific equipment is involved. Therefore, the CMOS Technology Roadmap is a key element permitting the entire industry anticipation and consequently a smooth pursuit of the Moore's laws. Predictive modelling and simulation are the main instruments for the conception of the Roadmap. However, the challenge for being predictive is very high today. This is because after 40 years of domination of the planar bulk transistor structure, starting from years 2000 a multitude of non-classical structures, non-classical materials, and non-classical technologies has come to play, Fig. 3. In addition, the physics governing the functioning of these devices changes. The device electrostatics changes (due to smallness of geometry), transport becomes ballistic or semi-ballistic, the quantum and confinement effects grow, mobility is strongly affected by mechanical strain (intentional or non-intentional), etc, etc. All these phenomena, being long time objects of academic studies, now become an engineer every-day task. Therefore, we not only need reliable and sophisticated models but we also need the models to be simple and implemented in a very different to traditional environment. An example of such can be the MASTAR [1] tool that in spite of having implemented sophisticated transport models, see Fig. 4, as well as confinement and strain physics, guaranties a push-button solutions to process and device engineers. Thanks to that hundreds of hypothesis and options could have been quickly evaluated with MASTAR when designing the ITRS CMOS roadmap.

CMOS FUTURE – BEYOND CMOS ?

The continuous scaling of CMOS transistors hits atomic resolution, thus menacing the CMOS future. As illustrated in Fig. 5, in an 8nm transistor (already scheduled in the ITRS roadmap) merely a few dopants will be present under the gate. This will expose the transistor characteristics to large statistical fluctuations. The impact of the latter is simulated in Fig. 6, showing disappearing SNM (static noise margin) of SRAM cells. More generally, phenomena that used to be well described by continuum statistical models, exhibit more and more random and singular character. Still another issue arises from the fact that scaling reduces the volume of the materials constituting the active device body. Device properties thus become dominated by interfaces. Electrochemical properties of interfaces being different from volume ones, new models and new simulation approaches are needed. Whereas in the past continuum models used to satisfy process as well as electrical simulations, today MonteCarlo, Molecular Dynamics and Ab-initio calculations have to enter industrial R&D labs, see Fig. 9.

CONCLUSION

The demand for modeling and simulation is today growing exponentially and could also be qualified as a Moore's law.

ISBN 3-901578-16-1

REFERENCES

[1] MASTAR tool is freely available from the ITRS 2005 web site, http://public.itrs.net/HomeStart.htm#Models

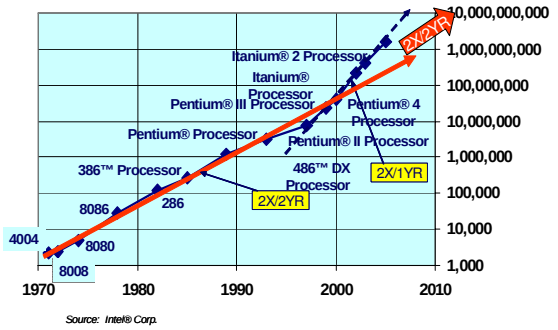

Fig. 1 Experimental CMOS transistors are hitting atomic resolution. Background graph copied from ITRS 2003.

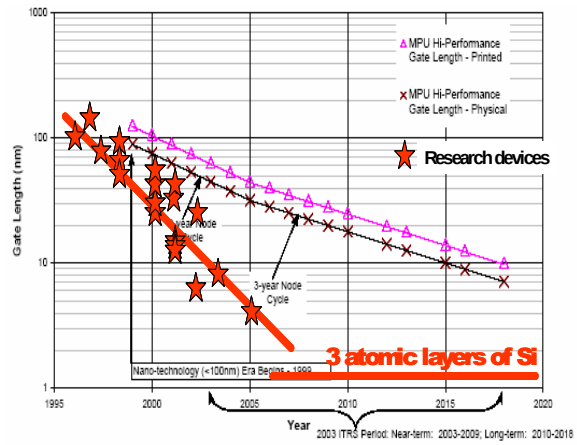

Fig. 2. Experimental CMOS transistors are hitting atomic resolution. Background graph copied from ITRS 2003.

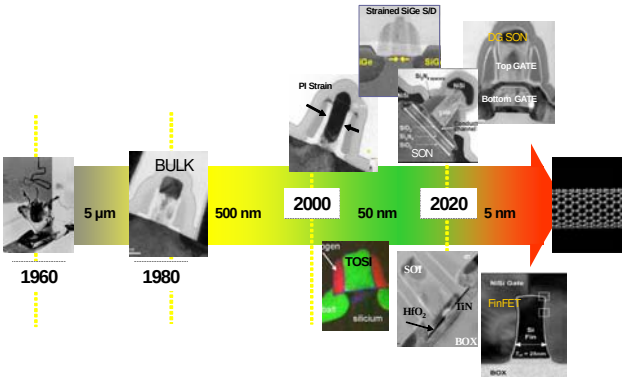

Fig. 3. Burst of non-classical CMOS device structures.

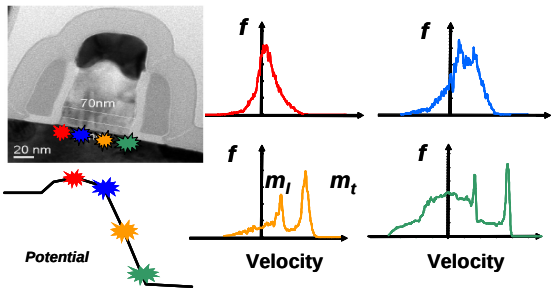

Fig. 4. Ballistic and semi-ballistic transport model by E. Fuchs, implemented in MASTAR.

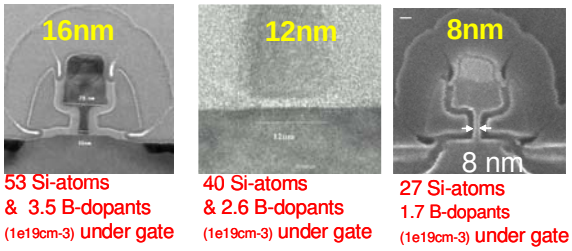

Fig. 5. Continues scaling reveals granularity of the matter.

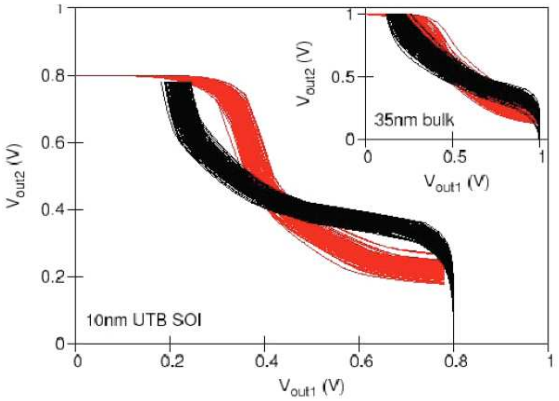

Fig. 6. Vanishing SRAM functionality with 35nm Bulk technology, and its recovering with UTB SOI, A. Asenov, SINANO Summer School, Glasgow 2005.

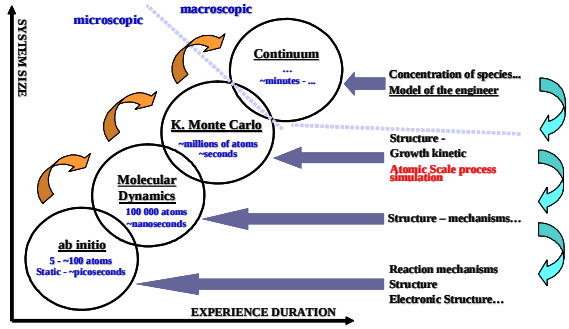

Fig. 7. Evolution of models used in IC industrial R&D.