Tracking the propagation of individual ions through ion channels with nano-MOSFETs

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The International Roadmap for Semiconductors (ITRS)[1] forecast that in 10 – 15 years the commercial transistor in semiconductor chips will reach sub 10 nm dimensions becoming comparable to medium size biologically important proteins like ion channels. Indeed completely functional transistors with 4 nm channel length have already[2] been demonstrated. Fig. 1 illustrates the atomic structure of a 4 nm double gate MOSFET in a close proximity of a Kcsa ion channel. The extreme sensitivity of such nano-transistors to stray charges[3] makes them suitable for sensing and interrogating charge configuration and transport in protein molecules. We have stipulated already[4] that the configuration in Fig.1 can be used to sense the current through an individual ion channel for high sensitivity bio-sensor applications. An array of addressable nano-MOSFETs could be used to map the distribution of ion channels in a living cell membrane and to monitor their movements. A combination of multilayered artificial membranes with imbedded ion channels in combination with underlying arrays of nano-transistors can be used in more complex sensing and pattern recognition applications, for new computing paradigms combining devices with electronics and ion transport and providing eventually links between electronics and molecular devices.

In this paper, applying drift-diffusion numerical simulations, we investigate the possibility to use a nano-MOSFET in a close proximity to an ion channel to study the dynamics of the ion permeation though the channel. The simulations are carried out using a commercial semiconductor device simulator with transport parameters fine tuned to represent both the electronic transport in the transistor and the ion transport in the solutions. The use of continuous drift-diffusion simulators to represent separately the transport though ion channel has already[5] been successfully demonstrated.

The sensing device is a double gate MOSFET with 4 nm channel length, 2 nm body thickness and 0.3 nm EOT. Figures 2 and 3 show the simulation structure and potential generated using Taurus[6] where the double gate transistor has had its top gate removed and replaced with an ionic solution containing a lipid membrane and a simple model ion channel pore. The I_d-V_g characteristics of the 5 nm double gate can be seen in Figure 4 with the top gate in place, with the top gate removed and[7] when the top gate is replaced by the ion-solution/channel system.

By placing an ion (represented simply as a single charge) (Figure 5) inside the pore we can measure the electrostatic effect of the passage of ions through the pore. Figure 6 shows the change in drain current as a function of charge position. Demonstrating that the presence of an ion in the channel is capable of modifying the behaviour of the semiconductor. Optimised experimental arrangements providing the best possible sensitivity for such measurements will be reported.

[1] International Roadmap for Semiconductors, the 2003 edition.

[2] H. Wakabayashi *et al.*, IEDM'03 Tech. Dig. 989 (2003)

[3] A. Asenov *et al.* IEEE Trans. Electron. Dev. 839 (2003)

[4] C.Millar *et al*, J. Comp. Elec, (2004)

[5] K.Hess *et al*, VLSI Design, (2001)

[6] http://www.synopsis.com

A full journal publication of this work will be published in the Journal of Computational Electronics.
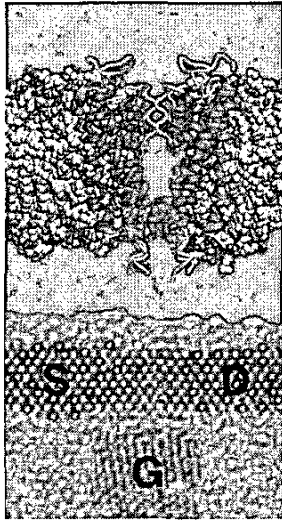
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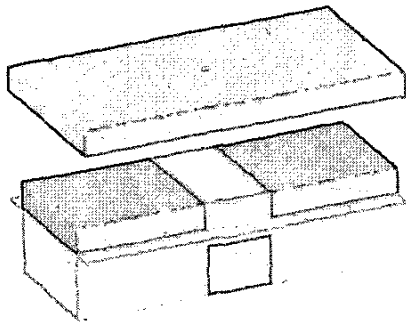Figure 1 : A Potassium Channel based on Kcsa as the second gate of a 5 nm doublegate MOSFET.

Figure 2: The Taurus simulation structure. The double gate transistor is shown at the bottom along with the lipid membrane and the small pore. Materials modelling water have been removed for clarity.
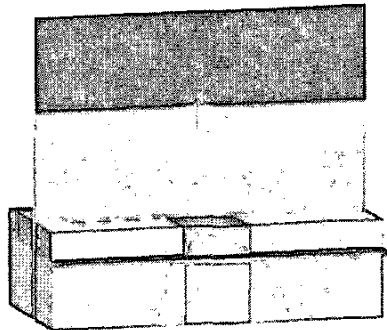

Figure 3: The potential profile through the Bio-Transistor for a drain voltage of 0.1 V and a bottom gate voltage of 0.2 V. A 0 V reference contact is positioned at the top of the simulation domain (not shown).
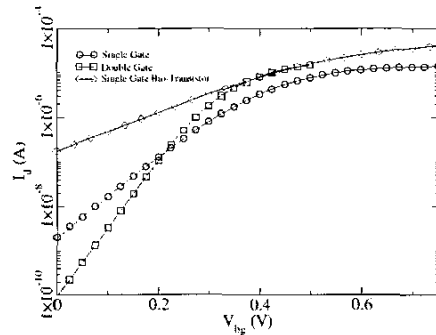

Figure 4: Id-Vg Characteristics of the 5 nm doublegate transistor, single gate and bio-gate configurations.
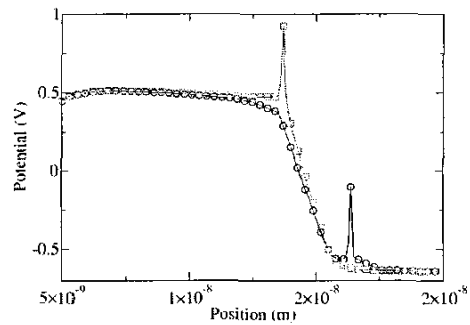

Figure 5: The potential profile through the channel and double gate in the presence of charges. Charges are placed at the top and bottom of the channel.
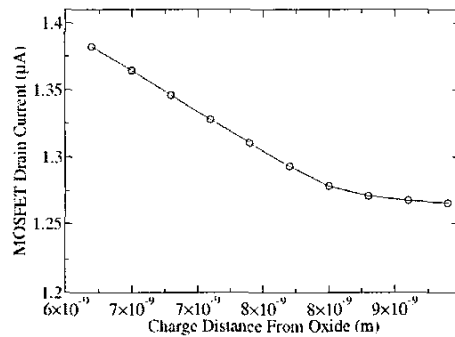

Figure 6: The effect of a single charge on transistor drain current. The charge is placed in the pore.

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