Simulation of Three-Dimensional Copper-Low-□ Interconnections with Different Shapes

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Interconnect plays a central for nanodevice, very large scale integration (VLSI), and system-on-a-chip (SoC). Investigation of interconnections will significantly benefit both the device fabrication technology and the VLSI SoC design communities [1]. Copper (Cu) has recently become a promising and popular material for the fabrication of interconnections. Unlike aluminum (Al) interconnects, the geometry of fabricated copper interconnects could be changed and deviated from the original structures. We in this work computationally explore the geometry effects on the parasitic elements of interconnect, resistance (R), capacitance (C), and time constant for RC delay [1-2]. For a given technology node, the geometry is explored with respect to a minimization of RC time delay. Optimal Cu-low-□ interconnect is significant and necessary for SoC era. It also benefits high frequency applications.

Evolution of VLSI design and manufacturing yields more faster and denser devices with ever-increasing functionalities. The continued downscaling of devices drives down the cost of SoC and makes its realization possible, but the complexity of design and manufacturing has consequently increased. In particular, it will be important for Cu-low-□ system. Advanced device technology improves transistor's performance, but the associated RC delay limits the performance [1-2]. VLIC's performance is dominated by the property of interconnects (wires). Therefore, design of interconnect parasitic elements becomes one of major challenge for SoC design. In this work, the geometry dependent RC time constant is studied for optimizing Cu-low-□ interconnects. Results show that the Cu-low-□ process can be subjected to further adjustment for minimizing unwanted time delay. Three simulated structures that they fabricated with cylindrical- (CL), square- (SQ) and rectangular-shaped (RE) wires, respectively, are shown in Figs. 1-3. Among them, the CL's case is interconnects with rounded corners. Metal lines with different length and spacing in realistic IC manufacturing are also examined. By solving three-dimensional Poisson and Laplace equations with adaptive computing technique [2], different structure's potential and electric field are analyzed, where R and C are simultaneously extracted [1-2]

Fig. 4 shows the extracted C from the three structures with different line space. The line widths of the three simulated structures are 90 nm and the height of the RE-shaped line is 180 nm. The extracted C decreases with respect to the line space, where the CL-shaped wire has the lowest C. It converges and saturates when the line space > 80 nm for all structures. Shown in Fig. 5, it is found that the RE structure has the lowest RC delay for the line width < 110 nm. The parasitic capacitance of the RE's case strongly depends on the width of metal line, thus the resistance lowering is minor and becomes insignificant. The RE-shaped wire is an attractive structure for the narrow wire, where the line width < 100 nm). However, from the fabrication point of view, the height of lines should be considered. Shown in Fig. 6, we can observe that the time delay tends to a constant when the line height > 160 nm.

The Cu-Low-□ metal lines have been explored with different shapes. An adaptive finite element simulation has been developed for the corresponding 3D models. The RE-shaped lines with the width in minimum size and a height about 180 nm may provide an optimal condition for 90 nm technology node.

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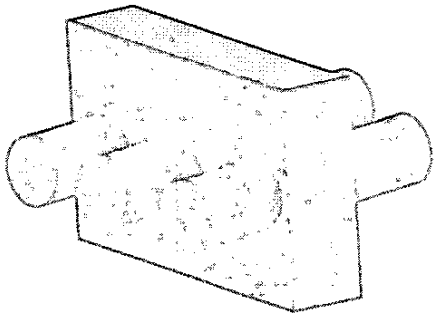

Figure 1: A 3D view of the cylindrical - shaped copper-low-□ interconnects.

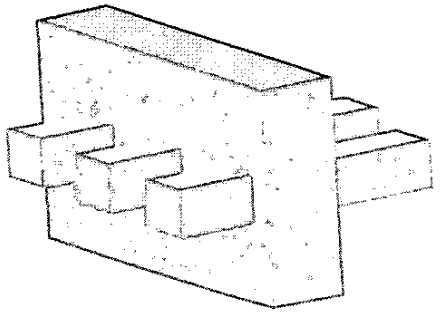

Figure 2: A 3D view of the square - shaped copper-low-□ interconnects.

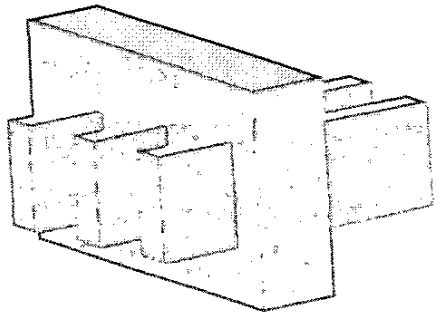

Figure 3: A 3D view of the rectangular - shaped copper-low-□ interconnects.

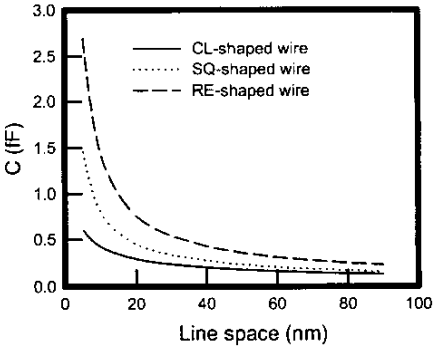

Figure 4: The calculated parasitic capacitance for the three interconnects with different line space.

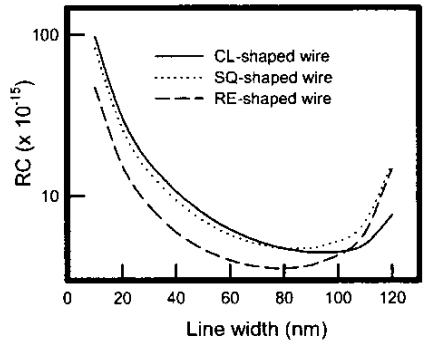

Figure 5: The RC time delay calculated for the three interconnects with different line width.

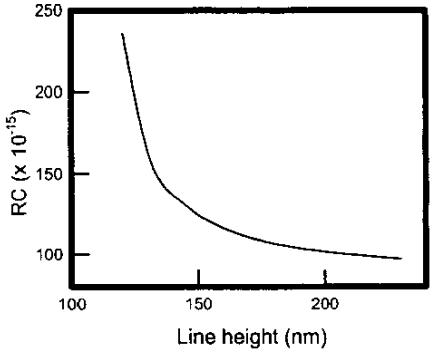

Figure 6: RC time delay of the RE-shaped interconnects with different line height.