A Unified Modeling of NBTI and Hot Carrier Injection for MOSFET Reliability

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A unified theory of Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) induced interface trap generation is developed to simultaneously explain the time-exponents of both phenomena. Characteristic time-dependence of interface trap generation ($\Delta N_{IT} \sim t^{n}$) due to NBTI ($\sim t^{0.25}$) and HCI ($\sim t^{0.5}$) degradation are shown in Figure 1a and 1b, respectively. Our model not only agrees with the experimental exponents and provides insight into dynamic behavior of the degradation processes for planar MOSFETs, but also predicts possible reliability concerns for the future-generation of surround-gate device geometries.

Although NBTI and HCI phenomena have traditionally been treated separately, in both cases Si-H bonds are broken at the Si/SiO_2 interface and hydrogen diffuses away from the interface leaving behind the dangling bonds that trap charges and shift transistor parameters. By exploring the geometry dependence of this Si-H bond breaking process, our model provides a fresh perspective that can resolve the fundamental difference between the theories of time exponents of NBTI and HCI, and it demonstrates that *it is the geometry, rather than the physics* of the individual mechanisms that determines the trap generation exponents.

The trap generation is simulated using the Reaction-Diffusion (R-D) model; the time behavior is initially governed by the competition between the breaking of the Si-H bonds followed by the release of hydrogen and the annealing of the broken bonds by the free hydrogen. In the second phase, hydrogen diffusion into the oxide begins to limit the interface trap density, giving the characteristic time exponents. Infinite surface recombination velocity is assumed at the oxide/gate interface. In NBTI, the active reaction region is uniform over the channel yielding 1-D diffusion, whereas HCI results in 2-D diffusion since the trap generation occurs only near the drain end (see Fig. 2a and b). Transient simulation is utilized to obtain the hydrogen density (N_H) in the oxide and the trap density (N_{IT}) at the interface as a function of time. The reaction at the interface and the hydrogen diffusion couple the neighboring nodes of N_{IT} and N_H.

It can be seen in Fig. 1c and 1d that the simulation results for time exponents under DC stress are in good agreement with the experimental data. Also shown in Figure 2c is the time exponents (n) for HCI from the literature. Despite the scatter in the data, the average value of n=0.5 is consistent with the prediction of the R-D model. Dynamic behavior is an important determinant of the realistic lifetimes of the transistors. In Figure 3, and similar to NBTI, our model can account for the stress and passivation cycles seen under AC bias and even the post-stress generation observed for HCI [1]. Additionally it explains why HCI relaxation is less compared to NBTI. Finally, our model implies worsened NBTI for surround gate devices like VRG, FINFET, and Si nanowire transistors. Figure 4 depicts the degradation for a cylindrical gate oxide. Decreasing the inner radius shifts the NBTI diffusion from 1-D to 2-D, with associated increase in N_{IT} generation.

To summarize, the unified R-D model describes in this paper successfully captures, for the first time, the geometry-dependence of trap generation and unifies HCI and NBTI. Significant achievements are: (i) agreement with the experimental data, (ii) realistic lifetime projection, and (iii) predictions of higher degradation rate for future generation of surround gate devices.

References: [1] D.S. Ang et al., IEEE TED vol.46, no.4 pg.738 1999. [2] G. Chen IRPS pg. 196 2003. [3] S. Mahapatra et al., IEEE TED vol.47, no.1 pg. 171 2000. [4] P. Heremans vol.32 no.12 pg.2194 1988. [5] R. Bellens IEEE TED vol.41 no.8 pg.1421 1994. [6] D.S. Ang IEEE EDL vol. 22 no.11 pg.553 2001 & EDL vol. 24, no. 9, pg. 598 2003. [8] Esseni IEEE TED vol. 49 no.2 pg.254 2002.

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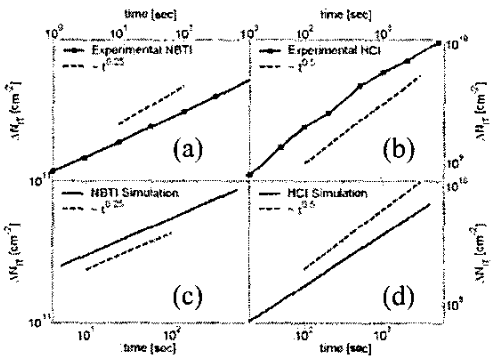


Figure 1: NBTI and HCI time dependence of interface trap density from the experimental data and the simulation results. (a) after [2], (b) after [3].

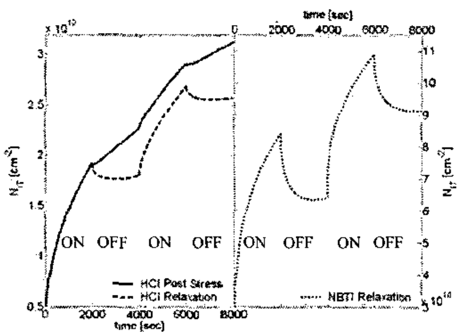


Figure 3: Stress and passivation cycles during the ON and OFF states of AC bias. The model predicts relaxation for HCI degradation. Post-stress trap generation reported in the literature can also be simulated.

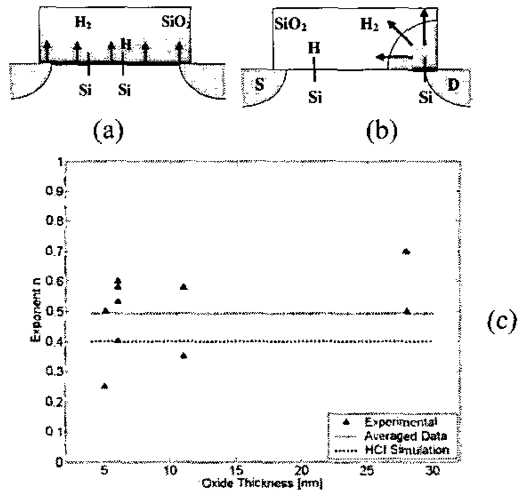
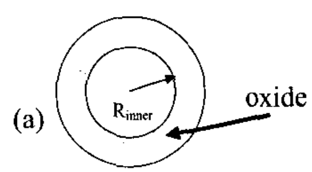


Figure 2: (a) Distribution of the interface traps in the channel and 1-D diffusion of hydrogen into the oxide for NBTI. (b) In HCI active trap generation is near the drain and the hydrogen diffusion is 2-D, source of the different time exponent. (c) HCI time exponents reported in the literature and the simulation exponent. Data are after [3-8] and averaged data are also shown.



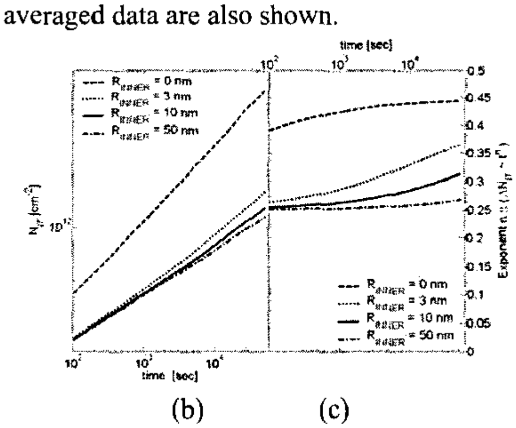


Figure 4: (a) Cross section of the cylindrical gate oxide. A planar oxide can be imagined as $R_{inner} \rightarrow \infty$. (b) Interface trap density increases for decreasing inner radius. (c) Time exponent and the hydrogen diffusion are NBTI-like for large radius. As the radius shrinks, the diffusion shifts to a HCI-like case and the time exponent increases. Higher NBTI degradation is expected for such device geometries.

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