Influence of Energy Transport Related Effects on NPN BJT Device Performance and ECL Gate Delay Analyzed by 2D Parallel Mixed Level Device/Circuit Simulation

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The consequences of energy transport related effects like velocity overshoot on BJT performance have already been studied previously (e.g. [1,2,3,4]). So far however most of the applied models were only 1D and it remained unclear whether such effects would have a significant influence on important quantities like ECL gate delay accessible only on circuit level. To the authors' best knowledge in this paper for the first time the consequences of energy transport related effects on the circuit level are investigated in a rigorous manner by mixed level device/circuit simulation incorporating full 2D numerical hydrodynamic models on the device level. To evaluate the influence of energy transport on bipolar transistor (BJT) performance a down scaled transistor structure with a base width of $50nm$ has been selected. This BJT is analyzed by the general purpose 2D hydrodynamic (HD) simulator GALENE III [5, 6] which incorporates besides the transient drift-diffusion model (DDM) a transient bipolar extension of the generalized HD model (GHDM) [7]. The latter model has been proven to reproduce Monte Carlo results very well [8].

For this down scaled structure the energy transport related effects on the device level are summarized in figures 1 to 4. Fig. 1 shows a significant velocity overshoot inside the base and collector space charge regions in the case of the HD model. On the other hand in fig. 2 it is shown that despite the velocity overshoot the DD collector current is larger than the HD one. This latter effect on collector current is caused by the thermal diffusion component in the GHDM, since it turns out that the difference in collector current nearly vanishes if the thermal diffusion component is significantly reduced. This influence of thermal diffusion can be understood by analyzing the directions of the two electron diffusion current components in the GHDM within the base region near the emitter. In this region the thermal diffusion component and the diffusion component driven by the gradient of electron density have opposite directions. This reduces electron injection into the base in comparison to the DD case.

Since HD simulations show that holes remain close to thermal equilibrium inside the emitter and base regions, the influence of the HD model on the base current is negligible (fig. 2). As a result the HD model yields a lower DC current gain (fig. 2) which is in good agreement with [3]. A smaller current gain tends to reduce the common base transit frequency f_T whereas velocity overshoot tends to increase it because it reduces base transit times. It can be seen in fig. 3 that both energy transport related effects on f_T nearly compensate each other, because very little difference between the f_T versus I_c curves resulting from both models can be observed.

The only significant difference observable in fig. 3 is that in the HD case $f_{T,max}$ is reached at somewhat larger collector currents caused by a delayed onset of performance degrading effects like high injection, base push-out and Kirk effect in the GHDM. The reason for this shifted onset is, that for a given collector current the peak HD electron densities are lower in the base and collector space charge regions than those resulting from the DDM. This is due to the velocity overshoot of the electrons and the larger lateral spreading of the electron density distribution (fig. 4). The increased spreading is a result of the elevated electron temperature in the collector space charge region which yields a higher electron diffusivity in the GHDM.

The consequences of the different energy transport related effects observable on the device level are difficult to access on the circuit level. To overcome this situation the mixed level device/circuit simulation system GALENE III/ CEDUSA has been established to study HD modeling effects on the circuit level without introducing simplifying assumptions on the device level like in the case of analytical models. The ECL inverter circuit analyzed by this simulator system is given in fig. 5. The circuit simulator CEDUSA allows to perform the GALENE III device simulations for the four BJT's within this circuit in parallel [9], which decreases the required CPU-time drastically. Fig. 6 shows the transient response functions V_{nout} at the inverter output after applying the ramp V_{inp} at the inverter input with the inverter being in steady state before. It can be seen that no significant difference exists between the two response functions and that especially ECL gate delay based on these results will be nearly identical for the DDM and the GHDM.

Though energy transport related effects are clearly visible on the device level their influence on circuit level quantities, e.g. ECL gate delay appears still to be insignificant even for devices which are scaled down beyond state of the art. This implies that presently and in near future there seems to be no urgent need to abandon the DDM for the optimization of ECL circuit performance. For the modeling of hot carrier effects [4] and device reliability the answer may be different however.

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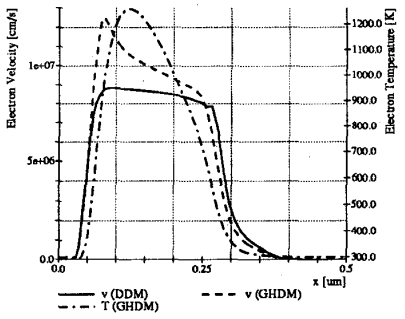

Figure 1: Electron temperature and velocity within intrinsic transistor at $V_{BE} = 0.8V, V_{CE} = 1.4V$

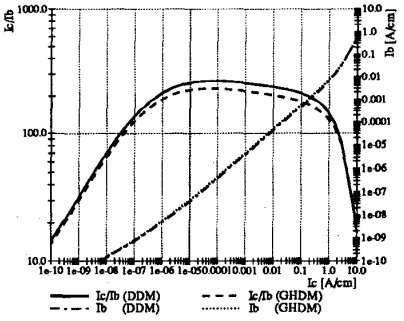

Figure 2: Gain I_C/I_B and I_B at $V_{CB} = 1V$

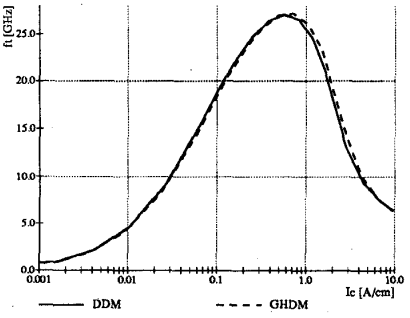

Figure 3: Common base f_T at $V_{CB} = 1V$

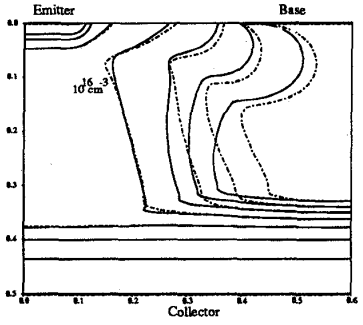

Figure 4: Plot of electron density equiconcentration lines for $V_{CB} = 1V$, $I_C = 0.73A/cm$ and the different device models (neighboring lines differ by a factor of 10; drawn line: DDM; dashed dotted: GHDM)

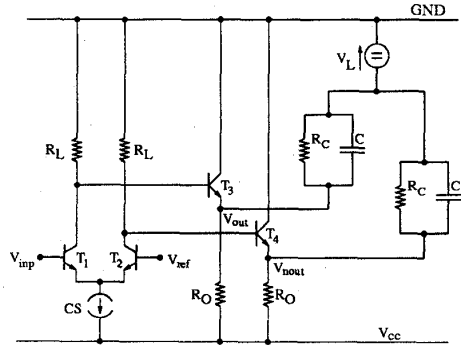

Figure 5: ECL-inverter circuit: $V_{CC} = -3.3V$, $V_{ref} = -1.087V$, $V_L = -1.087V$, $CS = 0.6mA$, $R_L = 0.672K\Omega$, $R_O = 4.036K\Omega$, $R_C = 95.7K\Omega$, $C = 14.2fF$

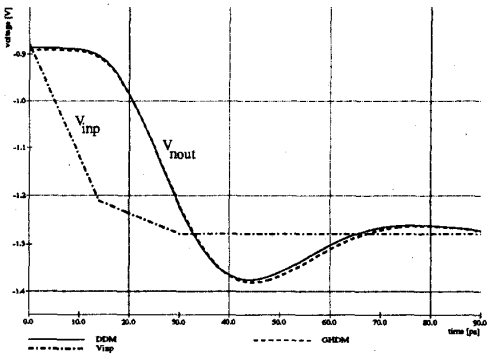

Figure 6: Transient response functions V_{nout} to the applied voltage ramp V_{inp}