Efficient Deep-Submicron Flash-EPROM Device Simulation Using Energy Transport Model

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In this work, we introduce a discretized-gate-capacitor (DGC) EPROM model and a post-processing quasi-transient (PPQT) method for efficient simulations of the programming and erasing of nonvolatile memory devices. The DGC model and PPQT method have been implemented in a 2D device simulator–UMDFET2[1] which solves a 2D Generalized Energy Transport (G-ET) model self-consistently, and includes impact ionization, hot-electron gate-injection, Fowler-Nordheim tunneling and Band-to-Band tunneling. This integrated efficient method requires one order of magnitude less CPU time than conventional methods[2, 3] as used in commercial simulation software, and is very accuracy. This method has been used in the design and optimization of deep-submicron Flash/EPROM devices.

The DGC EPROM device model shown in Fig. 1 uses many small discretized gate capacitors $C_f(i)$ defined by numerical mesh to take into account the interface potential variation $V_i(i)$, so the floating gate voltage V_{fg} can be accurately determined. This model also uses a "virtual control gate" and a control gate capacitor C_{cg} to replace the physical inter-poly dielectric structure. The 3-D gate coupling effect of the Poly 1 and Poly 2 overlap on the field oxide can thereby be effectively taken into account, and the treatment of the charge boundary condition is simplified. This DGC EPROM model combines the accuracy of the physical device model and the efficiency of the analytical device model. It requires much less CPU time and has better analysis ability than that using a full physical device model. It also have the flexibility for post processing,

In order to simulate the V_t shifting during the programming and erasing operations, the steady state solutions were first calculated to determine the initial threshold $V_t(0)$, the interface potential $V_i(x)$, and the gate current I_g as a functions of V_{fg}, which 15 to 20 minutes CPU time on SUN/SPARC2. It then took less than 1 second of CPU time using PPQT method to obtain the $V_t(t)$ shift curves shown in Fig. 3 for programming, and in Fig. 4 for erasing. The main advantage of the PPQT method is that it performs the steady state device simulation only once. The effects of different C_{cg}, initial charge on floating gate, different control gate voltage V_{cg} and arbitrary programming/erasing time can be easily calculated within a second.

The accuracy of deep-submicron device simulation has been verified by using 2D G-ET model[1], which is able to accurately calculate the velocity overshoot, hot-electron energy, and the impact ionization generation rate. The gate current was calculated by a modified Richarson's hot-electron injection formula, in which the Maxwellian exponent is replaced by the more realistic electron energy distributions based on Monte Carlo (MC) calculation. Fig. 5 shows the obtained excellent agreement between the calculation and the data from the indirect measurement method.

The summary results shown in Table 1 demonstrate that the electrical characteristics of EPROM devices with L_{eff}=0.25 and 0.45 μm were predicted with better that 90% accuracy on average by UMDFET2 which was only calibrated to devices with L_{eff}=0.35μm. It requires only about 20 minutes CPU time to evaluate each device. This great efficiency has enabled us to finish, in a short time, a large number of factorial simulations for the design and optimization of EPROM devices.

References

[1] Zezhong Peng, Ph.d dissertation of 1992, University of Maryland.

[2] T. Urai *et al*, *Electronic Letters*, Vol.26, No.11. May 24, 1990.

[3] S. Keeney,*et al*, *IEDM*, pp.201-204, 1990.

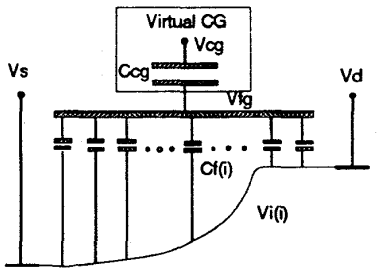

Figure 1: The discretized gate capacitor EPROM model, where the Cfg(i) is defined by numerical mesh of device simulation, and the "virtual control gate" is not physically simulated by numerical device simulation.

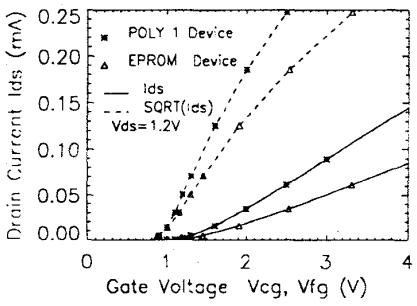

Figure 2: Calculated threshold characteristics for both Poly-1 and EPROM devices with L=0.5μm.

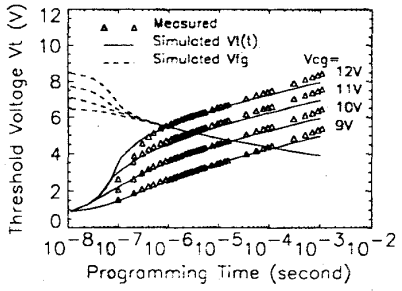

Figure 3: Calculated and measured programming characteristics $V_t(t)$ for a 0.5 μm EPROM device. It took only 1 second CUP time on Sun SPARC2 to calculate these four curves using the PPQT method.

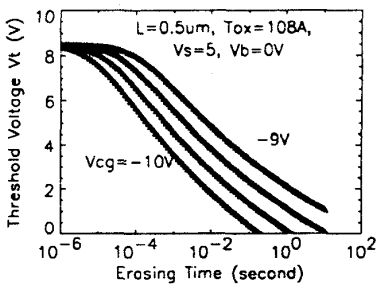

Figure 4: Calculated erasing characteristiecs for a 0.5μm Flash EPROM device.

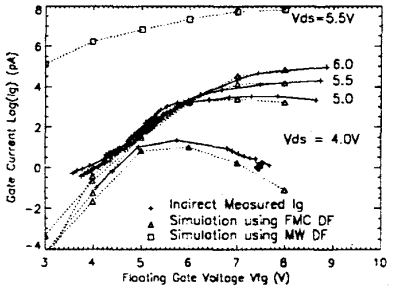

Figure 5: Calculated and measured gate current I_g for 0.5μm EPROM device. Excellent agreement to the measured data has been obtained by using a fitted Monte Carlo (FMC) electron energy distribution function, while the results using original Maxwellian (WM) distribution are more than three orders of magnitude higher than the measured data.

Table 1: Normalized summary results of EPROM Device Simulation

S/M	$Leff = 0.25\mu$	0.35μ	0.45μ
V_{t-p1}	1.02/0.87	0.98/1.0	1.02/1.02
$V_t(0)$	0.94/0.80	0.97/1.0	0.95/1.05
I_{dsr}	1.05/1.40	0.97/1.0	1.02/0.79
$dV_t(10\mu s)$	1.05/1.55	0.98/1.0	1.10/0.87
I_{ds-p1}	0.96/1.40	1.02/1.0	1.02/0.79
I_{sub-p1}	0.93/3.1	1.03/1.0	0.92/0.59
BVdss	0.99/0.76	1.11/1.0	1.16/1.18

Where "M" is for the measured data normalized by data for $L_{eff} = 0.35\mu m$, "S" for the simulation results normalized by the measured data, V_{t-p1} for Poly-1 device V_t, and $V_t(0)$ for initial EPROM V_t, I_{ds-p1} and I_{sub-p1} are drain and substrate currents of Poly-1 devices at $V_{ds} = 6(V)$ and $V_{gs} = 7(V)$ respectively.