A New Multilevel Simulator for MOS Integrated Circuits

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Introduction: Among the methods devised in past for nonlinear equations solution and adopted in a general-purpose circuit simulator the Newton-Raphson (NR) algorithm is one of the most used [1]. However, as good initial approximation of the roots to be found are not known *a priori*, the sequence of values produced by the algorithm will usually experience wild oscillations from one iteration to another, hopefully leading to convergence at the solution point. These abrupt changes during the NR iterations lead to slow convergence or possibly numerical overflow, and are mainly induced by the numerical propagation of externally applied voltage values, which define the boundary conditions for the system to be solved. In fact, before the effect of the externally applied voltage reaches the inner parts of a circuit, the latter are subjected to unrealistic local boundary conditions, which may not be well defined at physical model level. In particular, in MOS circuits we observed that source-bulk and drain-bulk junctions can become forward-biased during the simulation and lead to extremely high device currents, and, consequently, to the aforementioned problems.

In this work we present a new *MU*ltilevel *S*imulator for the analysis and design of MOS *I*ntegrated *C*ircuits at the device level (*MUSIC*). The input format is fully compatible with SPICE and eliminates the numerical overflow and slow convergence problems, due to numerical propagation of externally applied node voltages. We focus our attention on long chains of NMOS inverters, that, as already reported [2, 3] are quite difficult to simulate with existing techniques.

Some simulation problems with Spice3: An example of a basic cell is shown in Fig. 1, as is the complete test circuit type that can be made by replicating this cell N times. We added a few lines of code to the inner loop of Spice3 that evaluates the nodal voltages of the linearized circuit, to obtain the vector of nodal voltages after every NR iteration.

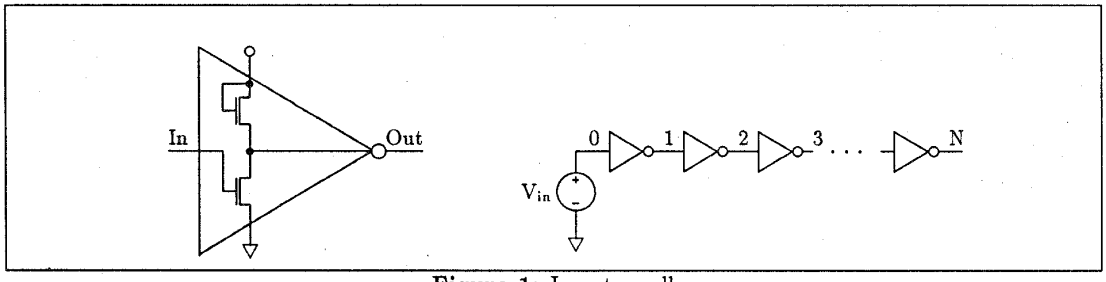

Figure 1: Inverter cell

Fig. 2a shows, in a semilog scale and for 33 inverters in the chain, the behaviour of the maximum node-voltage spike against both the inverter location in the chain and the current NR iteration step. The input voltage was kept constant at 100 mV above threshold, which was found to be one of the most difficult bias points to simulate. As can be seen, hasty oscillations occur during the first iterations. Similar behaviours were found in most of the examined circuits. The above data emphasize that the problem with the NR method lies in the propagation of the information regarding nodal voltages through the inverter chain. In fact, the output voltage of the last inverter cell takes far more iterations to converge than the first ones. Multilevel simulation addresses this issue by decomposing the circuit to be simulated into subcircuits, thus confining the scope of NR algorithm.

MUSIC multilevel simulator: Several approaches have been followed in the past to exploit the hierarchical decomposition of circuit equations. Hierarchy can be applied at different stages of the simulation. If it is used at the nonlinear equation level, it leads to the so-called MultiLevel Newton Algorithm (MLNA) [4]. The implementation of this procedure, which was done in an earlier version of our code MUSIC, evidenced that the MLNA is not particularly well suited to simulate hierarchical MOS circuits. This, in our opinion, is mainly due to the unilateral nature of MOS transistors. Additionally, it was also recently observed [3] that the damped NR algorithm can give rise to an increased convergence rate if a prioritization scheme is adopted in the selection of the equations to be solved.

MUSIC algorithm differs from the known MLNA, where during a subcircuit simulation all the terminals are kept at a fixed voltage, because subcircuit terminals are partitioned into two groups. The first one contains terminals either connected to voltage sources or terminals whose node voltage has already converged after a previous subcircuit simulation and therefore are kept at a constant voltage. The second group contains all remaining terminals, which are the "output" nodes of the subcircuit, where the local NR algorithm has to find the voltage solution. The load connected to these "output" nodes is the whole circuit except the subcircuit itself. The whole circuit, considered as load of the subcircuit, is modeled as a single device, calculating its companion model at the previous NR iteration. In this way we ensure that nodal voltages can reach their final status without enforcing unrealistic values, thus, they are allowed to follow their natural evolution in the discrete time defined by the iterations of the NR algorithm.

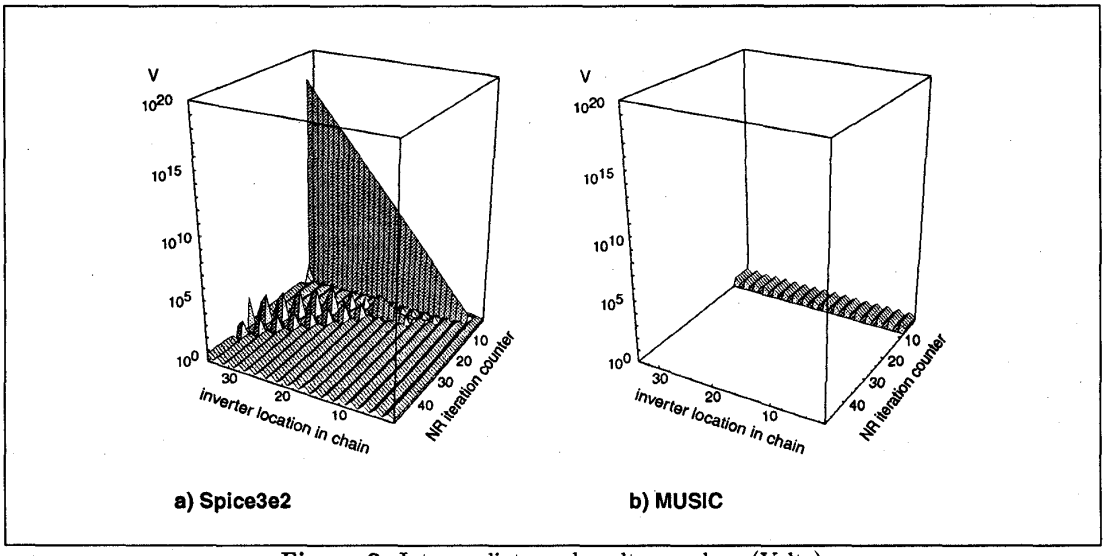

Figure 2: Intermediate node voltage values (Volts)

Fig. 2b shows a plot similar to that of Fig. 2a for simulations performed with MUSIC (N = 33). As it can be seen, the maximum voltage spikes are lower than 16 order of magnitude with respect to those found with Spice3 in Fig. 2a. Additionally, also the number of NR iterations and the CPU times were significantly reduced with respect to those found in Spice3. Finally, the following Table compares, for Spice3 and MUSIC simulations, the maximum magnitude of the node voltages u_i achieved during the iteration process and the number of iterations N_i required to reach convergence, for several numbers N of inverters in the chain.

N		5	11	33	55	77	101
Max $\|u_i\|$	Spice3	232 V	$5 \cdot 10^5$ V	$7 \cdot 10^{17}$ V	$6 \cdot 10^{27}$ V	10^{42} V	$4 \cdot 10^{56}$ V
	MUSIC	5 V	5 V	5 V	5 V	5 V	5 V
N_i	Spice3	17	24	49	76	100 (+52 g_{min} stps.)	100 (+60 g_{min} stps.)
	MUSIC	6	6	6	6	6	6

As it clearly appears, the maximum voltage spikes achieved with MUSIC on internal nodes are not higher than the supply voltage (5 V). Additionally it should be noticed that in SPICE for high values of N the magnitude of the node voltages is so large that cannot be represented in a single precision floating point variable on many machines, thus leading to an overflow error and aborting the simulation itself.

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