NEW INSIGHTS IN OPTIMIZING CMOS INVERTER CIRCUITS WITH RESPECT TO HOT-CARRIER DEGRADATION

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Introduction

Although much research has been done at the device level concerning hot-carrier degradation, simulation at the circuit level has only recently begun with the advent of reliability simulators [1-3]. This paper describes new insights obtained from hot-carrier simulations of several inverter circuits using an in-house reliability simulator named HIRES (Hitachi Reliability Simulator), which is based on the reliability simulator developed in [3] ([3] experimentally verified in [4]). It is found that insertion-MOSFET-based designs used to reduce hot-carrier degradation may not improve reliability unless properly optimized. A methodology is presented to optimize inverter design to increase reliability without sacrificing performance when compared to the simple inverter.

Simulation Set-Up

Two well-used insertion-MOSFET-based configurations are shown in Figs. 1 and 2. Fig. 1 shows the cascoded configuration where the gate of the cascode MOSFET is tied to the input, while Fig. 2 shows the insertion MOSFET configuration where the gate of the insertion MOSFET is tied to an independent power supply V_{GSins} [5]. The blocks labeled PMOSFET devices and NMOSFET devices consist of one transistor of the specified type, respectively, except in the case of the insertion MOSFET NAND and NOR gates, which contain the appropriate series or parallel connection of MOSFET's. The input signal consists of a 1ns rise and fall time pulse with a 30ns period and 50% duty cycle, with maximum voltage equal to V_{cc} = 3.3V. Device parameters are taken from an experimental submicron LDD process. Actual NMOSFET dimensions are W_n/L_n = 20/0.7 and PMOSFET dimensions are W_p/L_p = 32/0.838 in microns. The nominal value for the intrinsic threshold voltage (V_{th} at V_{bs} = 0 and small V_{ds}) is 0.7V. Load capacitance is set at C_L = 0.787pF and is determined by calculating the load that would take 1ns to discharge from V_{cc} to 0.

Discussion

Fig. 3 shows the effect of changing the intrinsic threshold voltage V_{th} of the insertion MOSFET on the device lifetime of the driver and cascode MOSFET's for the cascoded inverter configuration of Fig. 1. Note that for the case where identical devices are used for the cascode and driver MOSFET's (as is true in general and represented by the rightmost point of Fig. 3), the lifetime of the cascode MOSFET does not differ much from that of the simple inverter that is designed with the same current drive; i.e. the cascode MOSFET does not reduce hot-carrier degradation at all. By analyzing the voltage waveforms, it is found that for this case, the cascode MOSFET experiences most of the output voltage. By changing the current driveability of the cascode MOSFET with respect to the driver MOSFET, however, a more equitable division of voltage can be achieved between the cascode and driver MOSFET's. This is accomplished by changing V_{th} of the cascode MOSFET in Fig. 3. Note that an optimum exists at $V_{th} \cong$ -0.91V, at which point approximately a factor of 10^9 improvement in lifetime can be achieved. Fig. 4 shows the effects of changing cascode MOSFET current driveability by changing its device width W_{cas} at the optimum V_{th} found in Fig. 3.

Fig. 5 shows the effects of changing the current driveability of the insertion MOSFET for the insertion MOSFET inverter by varying V_{GSins}. The same type of curve can be generated as for the cascode inverter - an optimum point is found at $V_{GSins} \cong$ 2.9V with a device lifetime improvement of a factor of 10^5. However, if the device width W_{ins} of the insertion MOSFET is changed (Fig. 6), lifetime for both increase as W_{ins} is increased, in contrast to the cascode inverter of Fig. 4, due to the differences in capacitive coupling between the two structures. By using a devices twice as wide for the insertion and driver MOSFET (such as the W_n = 20μm example shown here), an inverter with a 10^5 increase in reliability but with the same performance as a simple inverter with W_n = 10μm can be designed.

Fig. 7 shows the device lifetimes of the NMOSFET's for different signal combinations applied to standard two-input NAND and NOR gates not containing insertion MOSFET devices. Each signal combination is identified using the following abbreviations. The keyword OUTER refers to the device connected to either ground for NMOSFET or V_{cc} for PMOSFET's, and INNER refers to the device between the OUTER device and the inverter output. OF refers to the signal connected to gate of the OUTER device going low-to-high first, IF refers to the signal connected to the gate of the INNER device going low-to-high first, and S refers to both signals changing simultaneously. The general pattern found is that the greatest amount of degradation occurs for the transistor of which the gate voltage causes a change in the output voltage. Note that the level of degradation is about the same as that of the simple inverter (in contrast with [5]). Using the insertion MOSFET technique of Fig. 2, and by using the same optimization technique as in Fig. 5, a 10^6 improvement in lifetime can be achieved.

Similar behavior as shown here are obtained for various capacitive loadings and input rise and fall times, and these results will also be presented.

References

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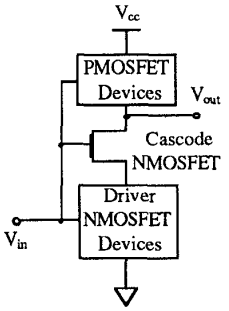

Fig. 1 General circuit schematic of the cascoded inverter configuration.

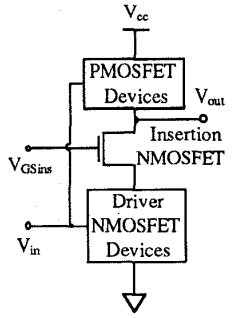

Fig. 2 General circuit schematic of the insertion MOSFET inverter configuration.

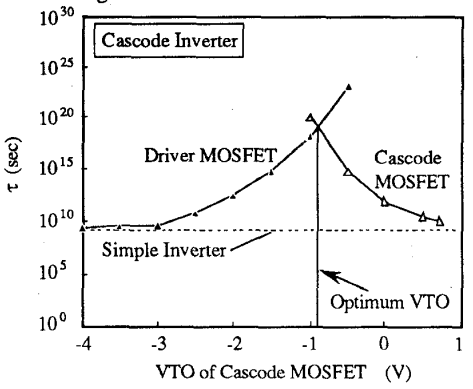

Fig. 3 Device lifetime τ of both NMOSFET devices versus VTO of the cascode MOSFET for the cascode inverter.

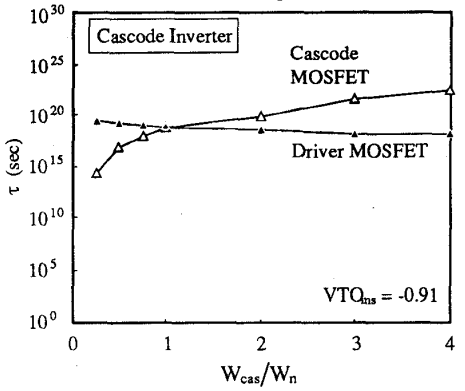

Fig. 4 Device lifetime τ of both NMOSFET devices versus W_{cas}/W_n for the cascode inverter.

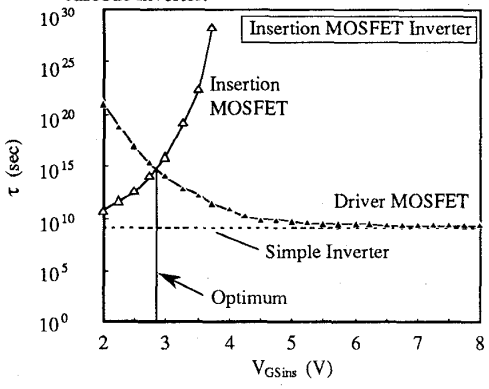

Fig. 5 Device lifetime τ of both NMOSFET devices versus V_{GSins} of the insertion MOSFET for the insertion MOSFET inverter.

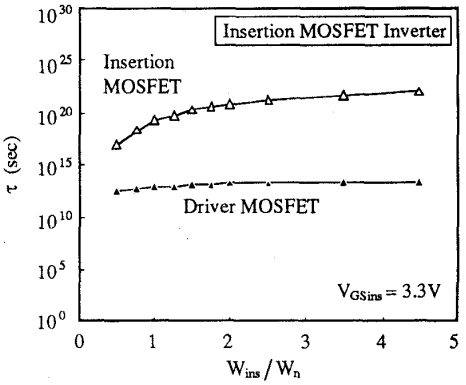

Fig. 6 Device lifetime τ of both NMOSFET devices versus W_{ins}/W_n for the insertion MOSFET inverter.

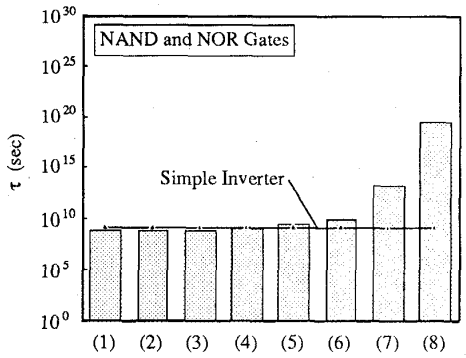

Fig. 7 Device lifetime τ for different input signal combinations for the two-input NAND and NOR gates.

Legend (see explanation in text):
(1) NOR NMOS connected to INNER PMOSFET, OF
(2) NOR NMOS connected to OUTER PMOSFET, S
(3) NOR NMOS connected to INNER PMOSFET, S
(4) NOR NMOS connected to OUTER PMOSFET, IF
(5) NAND INNER NMOSFET, OF
(6) NAND INNER NMOSFET, S
(7) NAND OUTER NMOSFET, IF
(8) NAND INNER NMOSFET, IF