Modeling and Simulation of Anomalous Degradation of Sub-um NMOS's Current-Driving due to Velocity-Saturation Effect

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1. Introduction

One of the vital issues for high-speed VLSI is current driving ability of component devices. Historically, a simple scaling-down approach has been believed to enhance the MOS device performance as well as to achieve high density VLSI. However, we found an anomalous degradation of submicron MOS device performance based on a study of intrinsic drain current which eliminates geometrical-effect and two-dimensional field-effect. It is noted that the degradation is observed on devices with channel length of 2.0 um. This paper describes modeling and simulation of the drain current degradation phenomena. A simple model which describe carrier-velocity-saturation is given to clarify the degradation, which leads to a good agreement with experimental Ids-L relationship in submicron NMOS.

2. Experiments and Numerical Simulation

It is well known that carrier-velocity-saturation is observed at drain region of MOSFET. However, in submicron regime of the device dimension, few discussions were given on how the phenomena affects device performance (current driving capability), since it has been measured and evaluated including its geometrical factor (W/L) and threshold lowering effect in short-channel structure. We found an anomalous degradation of the drain current in submicron devices as shown in Fig.1, which clearly exhibits performance loss in shorter channel NMOS when evaluating the normalized (W/L=1) drain current "Idso" at a constant effective gate bias (Ve=Vg-Vt) [1]. Note that the degradation occurs even for the device with L=2um at Vdd=5V, and lower Vdd cause a less performance loss in shorter channel devices. Fig.2 shows the same plot for a couple of devices fabricated in various technology levels. All the curves show an identical characteristics, showing a linear slope in Ids vs log(L) curves for L<2 um devices.

Numerical simulations of LDD-NMOS were conducted to evaluate field distributions along the channel for various channel-length devices as shown in Fig. 3. As demonstrated in the figure, lateral high-field is formed even at the source end in 0.3um NMOS, whereas the high-field region locates only near drain end in 1um NMOS. It is noted that the LDD N^- region works in lowering the field peak at drain region [2], however, it gives a small effect on field distribution in the channel. To clarify the effect of the distributed lateral field , field-strength is classified along the channel based on well known v-E curve (carrier-velocity-saturation) [3] as shown in Fig.4. The results are shown in Fig.5, indicating submicron NMOS's operate in weak and/or strong velocity-saturation condition along entire the channel region.

3. Modeling the Velocity-Saturation Effect

As discussed before, field dependent carrier-velocity is essential phenomena to model NMOS I-V characteristics. We newly formulated the effect taking into account the fact that weak velocity-saturation of the carrier dominates the carrier flow near source region as follows (see Fig. 4 & 5). From Fig. 4, we can assume the v-E relationship in weak velocity-saturation by the equation:

$$v = v_o \log\left(\frac{E}{E_o}\right) \qquad (1)$$

Based on boundary conditions with linear and strong-saturated regions as shown in the Figure, the parameters vo and Eo are derived in Eq. (2).

$$v_o = \frac{v_{sat} - \mu_o E_L}{\log\left(\frac{E_u}{E_L}\right)}, \quad E_o = E_L \left(\frac{E_L}{E_u}\right)^{\frac{\mu_o E_L}{v_{sat} - \mu_o E_L}} \qquad (2)$$

Since the drain current in saturation operation is calculated from lateral electric field and Eq.(1) at source end, the Idso for short channel (v-E weak-saturation relation) NMOS is formulated as:

$$I_{dso}(L_e) = C_o V_e \mu_o \left(\frac{E_L L_e}{\log(E_L/E_o)}\right) \log\left(\frac{V_e}{2aL_eE_o}\right) \qquad (3)$$

where, "a" is bulk charge factor [4]. Fig. 6 shows an experimental verification of the Idso degradation in shorter channel NMOS measured with devices fabricated using a 0.5um CMOS technology. Good agreement is obtained as shown in the Figure. Conventional plot of Ids(Ve=3V) vs L is also shown in Fig. 7, which indicates a empirical relationship of the Ids being proportional to $L^{-0.54}$. As shown in the Figure, the slope predicted from proposed model (Eq. (3)) coindides well with experimental data.

Details of the modeling and experimental verifications including PMOS characterization will be given.

4. References

[1] K. Tsuneno et al.: Tech. Paper of IEICE, SDM92-80, VLD92-55, pp. 41-47, Oct. 1992.
[2] Saitoh: Tech. Paper of IECE, SSD-78, 1978.

[3] S. M. Sze: Physics of Semiconductor Devices,p. 46, John Wiley & Sons, 1981.
[4] H. Masuda et al.: IEEE Trans. CAD, Vol. 10, pp. 593-597, Feb. 1991.

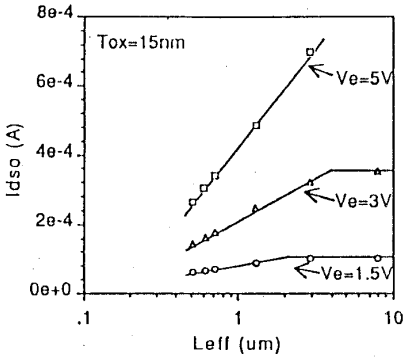

Fig1. Experimental Idso-Leff relationsip measured MOSFETs fabricated by a 0.5um prosess

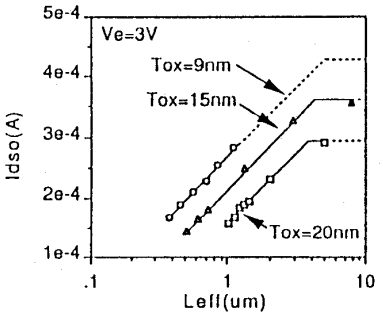

Fig2. Experimental Idso-Leff relationship obtained with devices fabricated by 0.2~1.3um prosess levels

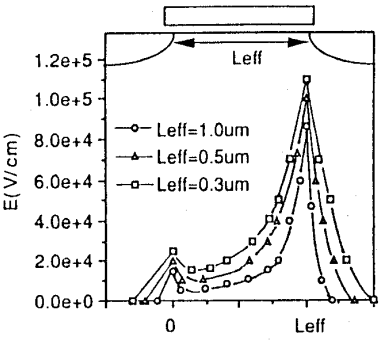

Fig3. Lateral field distribution analysys for Leff=0.3,0.5,1.0um MOSFETs

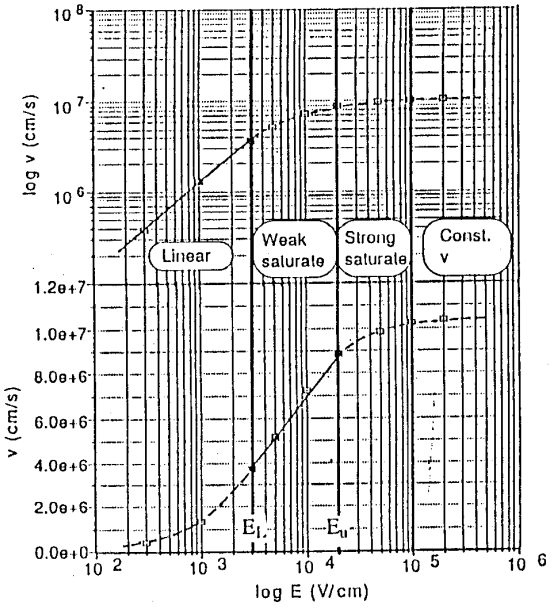

Fig4. Well-known v-E (logv-E) curve and its classifications

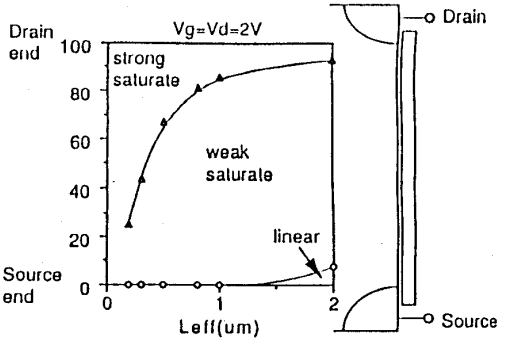

Fig5. Classified lateral field effects on the carrier(electron)-flow along the channel region

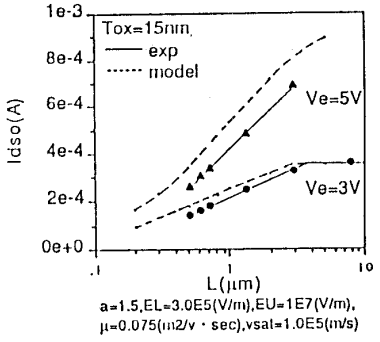

Fig6. Experimental verifications of Idso degradation in short channel stracture

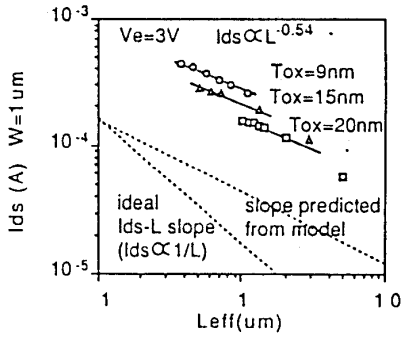

Fig7. Comparsion between experiments and proposed model on Ids(W=const.)-L curves