Analytical Surface Potential Expression for Double-Gate SOI MOSFETs

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Double-Gate SOI MOSFETs have been invoked to alleviate scaling limits of bulk MOSFETs. Since the potential distribution in these devices is quite unlike that in bulk MOSFETs, due to the symmetrical structure (Fig. 1) and extremely low doping concentration N_A [1], the models developed for bulk MOSFETs are not applicable. Using a perturbation theory, we solved the Poisson equation considering both depleted and induced charges, and derived an analytical expressions for surface potential, ϕ_S, for the entire subthreshold, moderate- and strong-inversion regions. We then derived analytical models for the threshold voltage, V_{th}, conducting charge concentration, Q_I, and subthreshold swing, S-factor (Table 1) which agree well with numerical and experimental data.

The surface potential is almost the same as the potential at the center, ϕ_C, and increases linearly with the gate voltage, V_G, in the subthreshold region (Fig. 2), which means that neither the depleted nor the induced charges contribute to the potential distribution. This feature is explained by Eq. 1 that the last component is much smaller than the others, reducing

$$\phi_S = V_G - V_{FB} - Q_{SI}/(2C_{Ox}).$$

When the induced charges do contribute to the potential distribution (meaning transistors switch on), the linear dependence of ϕ_S on V_G breaks down (Fig. 2). We found that $\phi_S - \phi_C$ has a substantial relation to the induced charges, and then defined V_{th} as the voltage at which $\phi_S - \phi_C$ is half the thermal voltage $1/\beta$, leading to a analytical expression for V_{th} (Eq. 2). We verified experimentally that this V_{th} gives a robust definition for the switch-on voltage (Fig. 3).

It must be noted that ϕ_S gradually increases from ϕ_{sth} at V_{th} as with increasing V_G even in the strong-inversion region. $\phi_S - \phi_{sth}$ is more than 100 mV at $V_G - V_{th} = 1$ V (Fig. 2). Our model readily expresses this feature and agrees well with the numerical data in subthreshold, moderate- and strong-inversion regions.

Q_I, which is calculated according to Eq. 4, is almost proportional to t_{SI} in the subthreshold region (Fig. 4), meaning that the entire channel regions contribute to Q_I.

Controversy exists as to whether volume inversion is expected with this device [2]. The volume inversion is not significant when t_{SI} is above 100 nm since Q_I depends weakly on t_{SI} at V_G of 1.5 V (Fig. 4). However, it becomes significant with decreasing t_{SI}. The volume inversion leads to a transconductance more than twice that of single-gate SOI MOSFETs at a given t_{SI}. However, t_{SI} should be designed as large as possible to obtain a high transconductance since Q_I monotonically decreases with decreasing t_{SI}. The upper limit of t_{SI} should be determined considering the punch-through limit [3].

The S-factor is determined solely by the surface potential and insensitive to ambiguous mobility model, and hence enables us to test our model stringently. The theoretical S-factor agrees well with the experimental data [1] in both the subthreshold and strong-inversion regions (Fig. 5). S-factor of this device has the ideal value of $\ln 10/\beta$ in the entire subthreshold regions, which is well explained by that the second component of Eq. 3 is much smaller than 1 when V_G is less than V_{th}.

References

[1] T. Tanaka et al., 1991 IEDM Tech. Dig., p. 683.

[2] F. Balestra, IEEE Electron Device Letters, vol. EDL-13, p. 658, 1992.

[3] R. H. Yan et al., IEEE Trans. Electron Devices, vol. ED-39, p. 1704, 1992.

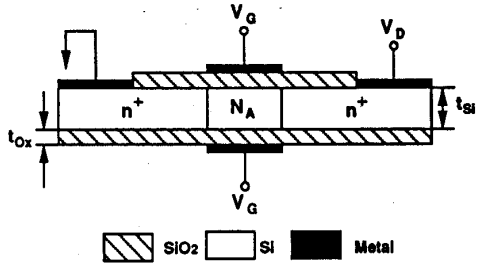

Fig. 1 Double-gate SOI MOSFET.

Table 1 Equations

$$(1)\quad \phi_s = \begin{cases} V_G - V_{FB} - \dfrac{Q_{Si}}{2C_{Ox}}\left[1+\gamma\dfrac{\left[1+\frac{1}{2}\left(1+\frac{4C_{Si}}{C_{Ox}}\right)\right]e^{-\beta(V_{th}-V_G)}}{1+\frac{1}{2}\left(1+\frac{4C_{Si}}{C_{Ox}}\right)e^{-\beta(V_{th}-V_G)}}\right] : (V_G < V_{th}) \\ \phi_{sth} + \dfrac{1}{\beta}\ln\left[\dfrac{1+\frac{\beta^2}{8}\left(\frac{C_{Ox}}{C_{Si}}\right)^2(V_G - V_{FB} - \phi_{sth})^2}{1+\frac{\beta^2}{8}\left(\frac{C_{Ox}}{C_{Si}}\right)^2(V_{th} - V_{FB} - \phi_{sth})^2}\right] : \quad (V_G > V_{th}) \end{cases}$$

$$(2)\quad V_{th} = V_{FB} + 2\phi_F + \frac{\ln\gamma}{\beta} + \frac{(1+\gamma)Q_{Si}}{2}\left(\frac{1}{4C_{Si}} + \frac{1}{C_{Ox}}\right)$$

$$(3)\quad S = \frac{\ln 10}{\beta}\left[1+\frac{1}{2}\left(1+\frac{4C_{Si}}{C_{Ox}}\right)e^{-\beta(V_{th}-V_G)}\right] : (V_G < V_{th})$$

$$(4)\quad Q_I = 2C_{Ox}(V_G - V_{FB} - \phi_s) - Q_{Si}$$

where $Q_{Si} = qN_A t_{Si}$; $C_{Si} = \dfrac{\varepsilon_{Si}}{t_{Si}}$; $C_{Ox} = \dfrac{\varepsilon_{Ox}}{t_{Ox}}$; $\gamma = \dfrac{4C_{Si}}{\beta Q_{Si}}$

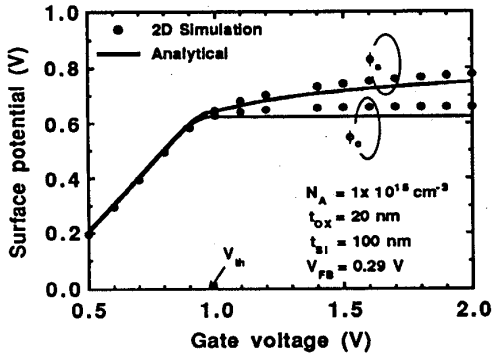

Fig. 2 Analytical and numerical potential at the center ϕ_c and SiO_2-silicon interface ϕ_s as a function of gate voltage.

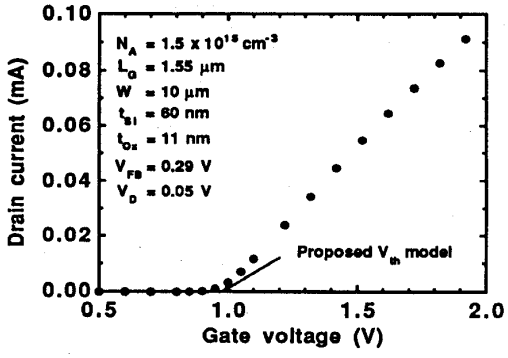

Fig. 3 Experimental V_G-I_D characteristics.

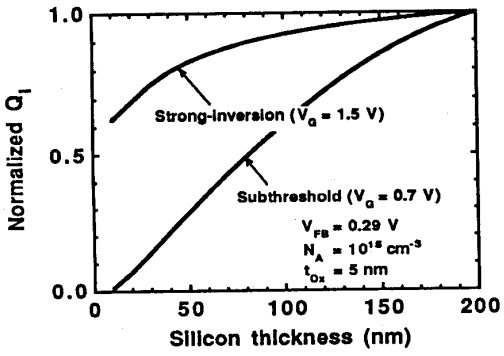

Fig. 4 Dependence of conductive charge concentration, Q_I, on silicon thickness. V_G of 0.7 V corresponds to the subthreshold region and 1.5 V to the strong inversion region.

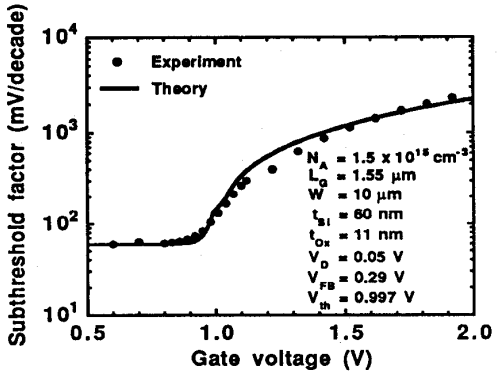

Fig. 5 Comparison of the experimental and analytical S-factor.