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MASTAR - a Model for Analog Simulation of subThreshold, saturation and weak Avalanche Regions in MOSFETs.

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The state of the art. There are at least three areas in MOSFET operation in which digital CAD models fail. The first is the subthreshold region, which has become of increasing interest for its potential in low power amplifiers, which are needed in rapidly developing portable communication devices. The second is the transition from ohmic to saturation region (problem of discontinuity in the output resistance $r_{out}=\partial V_d/\partial I_d$), and the third, the weak avalanche region, where the error in r_{out}, calculated with a digital CAD model, can attain 100% and more [1], which excludes analog applications of such a model.

The purpose of the work. The purpose is thus to develop models (package MASTAR) for threshold voltage (the same V_{th} model is to be used for drift and diffusion current calculations), subthreshold current, substrate current, and the transition region, which when added to any digital CAD model will extend the validity of the latter to subthreshold and analog applications.

MASTAR features, and results. MASTAR is derived using the VDT (voltage-doping transformation) technique [2] which has already been successfully used in CAD modeling e.g. in [3] and [4]. The present work is a continuation of [2] and [4] greatly simplified and extended so as to include all small-size effects known to date. The improvements are presented in more detail below.:

- all dependencies have been simplified so as to be simple and explicit functions of only applied biases and geometrical dimensions. Regarding the body effect, one single expression covers both small and large V_B biases. Automatically, the continuity of V_{th} and its derivatives as a function of V_B (lacking in many digital V_{th} models) is ensured. Nevertheless, the two-slope behaviour of the V_{th}-versus-V_B characteristic (corresponding to two - surface and bulk - body factors) is correctly accounted for, see Fig. 1;

- in spite of a common V_{th} formula for P-MOS and N-MOS transistors, their particularities are preserved (via different parameter values). As shown in Fig. 2(a) and 2(b), the two-slope behaviour of N-MOSFETs does not occur in our P-MOSFETs (buried channel), and the dependence of V_{th} on V_D (at V_B close to 0V) is much stronger for a P-MOSFET than a N-MOSFET, both effects being reflected by the model. Worth noting is also the high degree of accuracy at short channel and simultaneously high V_B and V_D biases (see Fig. 2), which is an important but rarely fulfilled condition for analog applications;

- the MASTAR package takes into account all small size effects known to date, i.e.: short and narrow channel effects, the DIBL effect, the junction depth effect, the OED (oxidation enhanced diffusion) effect [5], and the DICE (drain-induced channel enlargement) effect [6]. The manifestations (as measured and modelled) of the OED effect (N-MOSFETs) and of the DICE effect (P-MOSFETs) can be observed in Figs. 3(a) and 3(b), respectively;

- as illustrated in Figs 4(a) and 4(b), the variation in the subthreshold slope with applied biases (V_B and V_D) and geometrical dimensions is accurately predicted. The slope variation is especially visible in a short-channel P-MOSFET (Fig. 4(b)) which is generally more prone to short-channel effects than a N-MOSFET;

- a very important feature of the MASTAR is the threshold voltage dependence on drain bias V_D (DIBL effect) and the Enhanced Body Effect (EBE), arising from the self-biasing of the bulk by the substrate current [7]. The improvement in accuracy of calculation of drain current I_D and output resistance r_{out} (resulting from taking into account these effects) is illustrated in Figs. 5(a) and 5(b), respectively. The characteristics are calculated using a digital CAD model [8] accomplished by the MASTAR package. Note that, as regards I_D, the error at V_D=5V is reduced from 12% to 0.5%, and the error concerning r_{out} is reduced from 510% to merely 1.5%;

- another important finding of this paper is that because of the positive feedback between drain and substrate current (see [9]), the simple relation: $I_{sub}=MI_{dsat}$ where M is the multiplication coefficient, and I_{dsat} the saturation current (independent of I_{sub}), does not hold in the weak avalanche region. A new improved formulation, taking into account the positive feedback without introducing any implicit relation between I_{sub} and I_D, is proposed. In addition, we have simplified the EBE model [4] so as to end up with an additive term directly in the current expression ($I_D=I_{dsat}+const I_{sub}$) instead of passing through the V_{th} reduction. This simplification facilitates the extraction of parameters as well as an analytical calculation of r_{out}.

- in order to remove the discontinuity in r_{out} at saturation (inherent in many digital models), MASTAR replaces the V_{DS} voltage by a certain effective voltage $V_{DSX} = V_{DS}[1+(V_{DS}/V_{DSAT})^{\beta}]^{-1/\beta}$, as suggested in [10]. The positive result of this replacement can be observed in Fig. 5(b). In addition, a great improvement in the r_{out} calculation accuracy in the region from saturation to weak avalanche (see Fig 5(b)), is achieved by introducing a new term, accounting for the channel-length modulation, in the MASTAR V_{th} model.

- the parameters of the MASTAR package form a linear system, this having two important practical implications. The first is that all parameters can be extracted directly via specific measurements, without the need for optimisation on a whole set of parameters which is more CPU time consuming and less significant from the physical point of view. The second is that it is possible to turn-on or -off certain effects by simply putting the corresponding parameters to 0, thereby tailoring the MASTAR package to one's own technology.

Conclusions. The paper presents the CAD package MASTAR, together with the parameter extraction procedures (single set of parameters for a given technology). The package utility in analog and low power circuit simulation is demonstrated. The package can be used with almost all CAD digital current models, thereby extending their validity to subthreshold and analog applications. Recently, we have automated the extraction of parameters and incorporated the MASTAR in our ELDO circuit simulator where it works together with the digital model [8]. According to our estimations, the expense of this operation, in CPU time, does not exceed 30%, compared to simulations of the same circuits using the original digital model (without MASTAR).

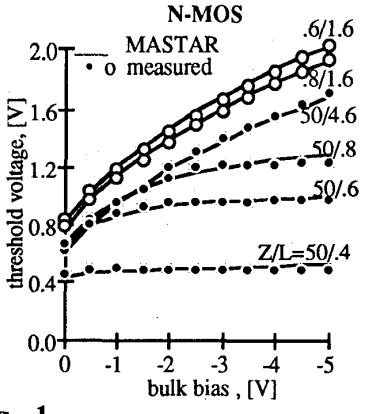

Fig. 1

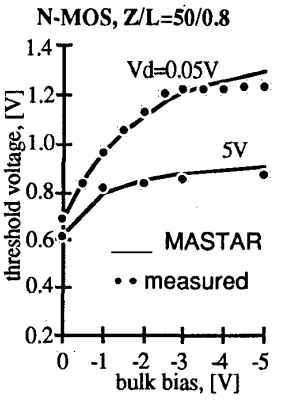

Fig. 2a

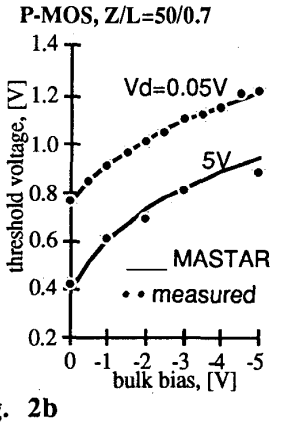

Fig. 2b

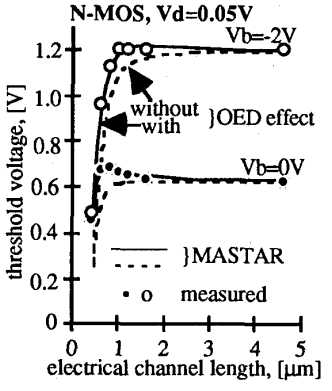

Fig. 3a

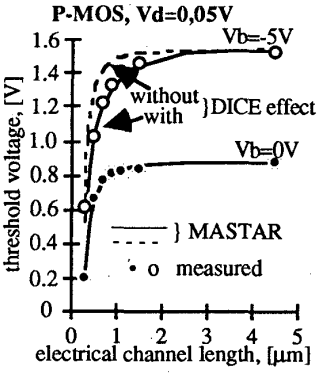

Fig. 3b

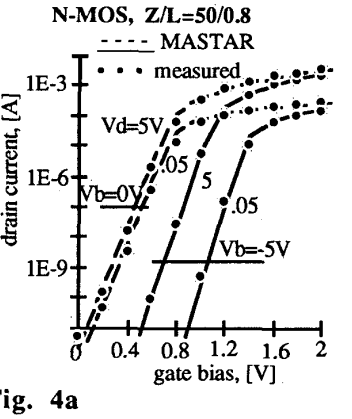

Fig. 4a

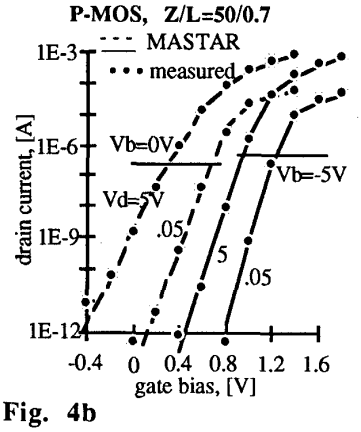

Fig. 4b

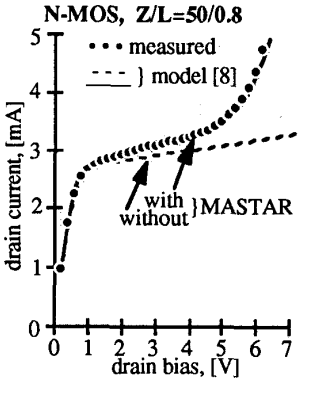

Fig. 5a

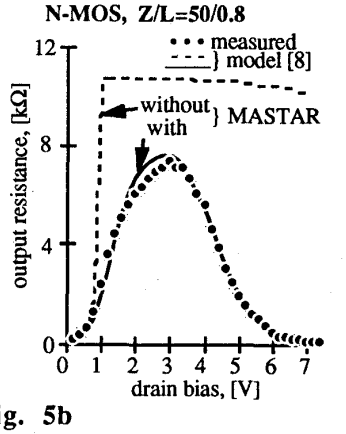

Fig. 5b

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