CAPACITANCE CALCULATION OF VLSI MULTILEVEL WIRING STRUCTURES

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Interconnection wiring is gaining a significant importance in speed of modern VLSI circuits. One of the reasons interconnections limit their performance is the wiring capacitance. With increasing chip dimensions, parasitic interconnection capacitances dominate the gate capacitance.

Nowadays, boundary integral methods are widely used to solve the numeric field computation problem for the energy calculation. The reduction of volume discretization to surface discretization is the main advantage of this method. The first disadvantage of the method is that it cannot be extended to nonlinear regions, i.e. materials with space charge. Material interfaces and homogenous Neumann boundary conditions result in a significantly higher calculation effort. To avoid those disadvantages, we have decided to adopt a variational formulation of the problem and use the finite element method. The minimized functional equals exactly twice the electrostatic field energy.

For a n – conductor problem we need $n\ (n-1)/2$ field calculation runs with different applied conductor potentials. A post processing tool solves a small linear equation system to extract the $n\ (n-1)/2$ partial capacitances in a charge balanced system. Due to the linearity of the Maxwell equations, one needs only n field calculation runs with an independent set of conductor potential vectors. With a simple superposition of the potential values from preceding runs, we get new equations to extract the capacitance matrix.

The discretization of the wiring structure is done by a transfinite interpolation [1] of the domains. The resulting elements are hexahedrons. To prevent numerical integration of the element stiffness matrices, we developed a special splitting algorithm under the restriction of upkeeping the right connectivity of the elements. First, the program tries to split up the element into five tetrahedrons. If this is impossible, the element is split up into six tetrahedrons, and as last possibility into twelve elements.

To achieve an efficient usage of computer memory, we developed a compressed matrix format for the stiffness matrix. Only the non–zero row entries are stored. Additionally, because of the symmetry of the equation system, only half of the matrix has to be stored. An index matrix holds the references to the column index in the stiffness matrix. To get an entry in the stiffness matrix, a binary search is used to find the column index in the index matrix [2]. The new implementation of a LU–preconditioned conjugate gradient solver which uses this special matrix format reduces computational time and memory consumption. The disadvantage of column searching is prevented by an intelligent algorithm design for matrix accesses in the solver and preconditioner part.

For the preconditioned solver, the method of Eisenstat [3] achieves a significant speedup, because the matrix vector multiplication can be reduced to a multiplication of a vector with a diagonal matrix. This new solver achieves a solver speedup relative to the formerly used CG Solver of the NSPSG Package [4] of a factor of five or more for calculated problems such as crossing wires structures. Vectorizable code is implemented in separate subroutines.

As an example, Fig. 1 shows the simplified wiring structure of a DRAM–cell. Only the boundary conditions are shown. The cell is repeated in a mirror–like fashion. The semiconductor area (1) is taken to be a ground plane. Above the ground plane (2) one can see the word –line and on the top two bit – lines (3,4). The cell layout size is approximately $1.2 \times 0.8 \mu m$. Fig. 2 shows the discretized domain – a tetrahedral grid. For the visualization of the potential distribution, a post–processing tool was developed. As a special feature, the visualized potential distribution within the elements has the same form as the element shape functions.

The first run (Fig. 3) was performed with a potential of $1V$ at contact (1) and all other contacts were set to $0V$. The second run (Fig. 2) with (2) to $1V$ and all other contacts $0V$. For this four–conductor problem, six partial capacitances are calculated from the six energy values:

$$C_{12} = 3.007\ 10^{-16}\ F \quad C_{23} = 2.158\ 10^{-17}\ F$$
$$C_{13} = 1.146\ 10^{-17}\ F \quad C_{24} = 2.230\ 10^{-17}\ F$$
$$C_{14} = 1.010\ 10^{-17}\ F \quad C_{34} = 5.178\ 10^{-17}\ F$$

The simulations were carried out on a DECstation 5000 and required 17 minutes CPU time.

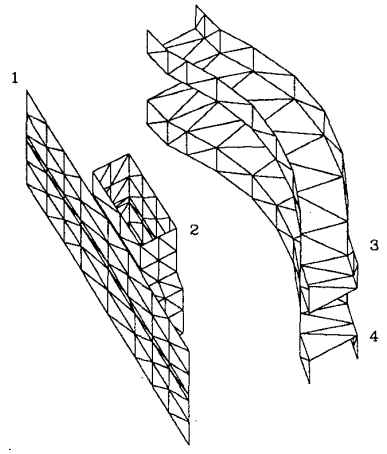

Figure 1: Simplified dynamic RAM–cell

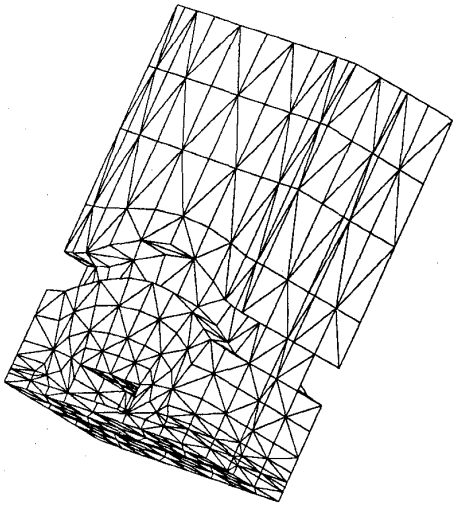

Figure 2: Tetrahedron grid, $\epsilon_r = 3.9$
2790 elements, 4991 nodes

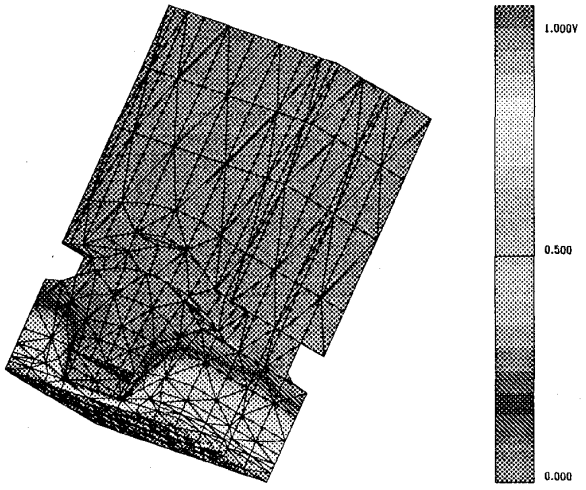

Figure 3: Potential distribution, run 1

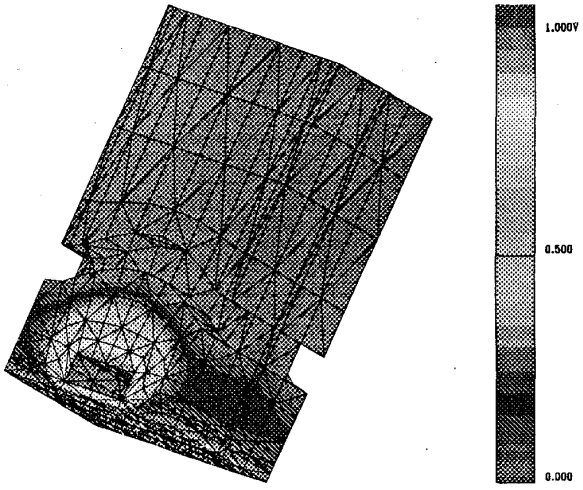

Figure 4: Potential distribution, run 2

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