A Consistent Drain and Substrate Current Model of LDD MOS Devices for Circuit Simulation

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Abstract - This paper describes a Spice-compatible circuit simulation model of submicron LDD MOS devices. It includes an enhanced model of our previous drain current characteristics *(UNIMOS)* and a new analytical substrate current model. For the drain current characteristics, new features of our previous model has been added for achieving good accuracy and convergency. In addition, the two-dimensional electric field distribution during impact ionization which has much more physical meaning is considered for developing the hot electron model. Thus, a new and accurate substrate current model is proposed based on the so called effective electric field, instead of the conventional peak electric field concept used by the lucky-electron (LE) theory. Comparison of the modeled results with those of experiment shows excellent match for a wide range of device channel lengths and bias conditions.

Introduction

In recent years, three basic models needed for circuit simulation in Spice are the dc(I-V), ac (C-V) and the hot carrier models. The first two MOS device models in Spice have been developed for years [1]. The Berkeley SPICE MOS models which have been evolved from LEVEL 1, 2 3 to a recent LEVEL 4- BSIM [2] version has shown wide applications for conventional MOS devices. However, the effort put on the hot carrier model is not sufficient [3]. It is also known that the substrate current,I_B, can be used for monitoring the hot carrier effect and also for analyzing the device or circuit hot carrier reliability in VLSI design. Owing to the limitation of the I_B model based on the conventional LE concept, a substrate current model is essential for developing or optimizing hot carrier resistant devices or circuits using Spice as an aid. Continuing efforts will be made to improve currently used dc models and the inclusion of the substrate current in circuit simulation using Spice.

In modeling the substrate current of a conventional MOS device, the following form [4] based on the Lucky-Electron concept is widely used:

$$I_B = \frac{\alpha}{\beta \cdot l_d} E_m I_D \exp(-\frac{\beta}{E_m}) , \tag{1}$$

in which $E_m=(V_{DS}-V_{Dsat})/l_d$ is generally considered as the maximum electric field within a device. The electric field inside devices is a complicated 2-D distribution and the substrate current should be the overall result of the field distribution. As a consequence, the surface peak electric field can not always accurately modeling the substrate current using (1), particularly for LDD-structure devices.

The present Spice model includes a consistent set of I_D and I_B models. An enhanced version of our previous I_D model will be first described. In addition, a new substrate current model based on the 2D effective electric field concept will be demonstrated.

Unimos-Plus: An Enhanced Submicron LDD MOS Device Drain-current Model

An enhanced version of the drain current characteristics of small geometry LDD MOSFETs was first developed based on our previous models in [3,5] and a newly-developed optimization algorithm. The expressions achieved for the drain currents hold in the weak inversion, strong inversion and saturation regimes of operation. Fig.1 shows the schematic diagram of an LDD MOS device, in which the device is considered to be an intrinsic MOS device in series with two voltage dependent drain-and-source series resistances. These two resistances are derived as functions of gate voltage and drain voltages. For the former, the total drain-and-source series resistance is characterized as functions of the gate voltages. For the latter, it has been incorporated into the mobility degradation term, eq.(A1), so that accurate I-V characteristics in the linear region can be achieved. In the device saturation region of operation, the determination of saturation voltage, V_{DSAT}, is rather important which will affect the accuracy of the I-V curves and also the continuity of these curves. Fig.3 shows the resultant V_{Dsat} at various gate voltages. Verification of the I-V model is given in Fig.4 which gives quite good match with experimental data. Discontinuity of the I-V curves at the near threshold region in the Spice LEVEL=3 has been solved by adding only two empirical factors α and I_0, as shown in eq.(A3), Table 1. Both parameters can be determined experimentally. Smooth transition at the near threshold (Fig. 5) is obtained which can speed up the convergence in circuit simulation and hence saves CPU time. Only *12 model parameters* are used to fully adapt the small geometry I-V models to a given process which is much less than the BSIM model. Benckmark test of a ring oscillator shows a 30% savings in CPU time by comparing with Spice LEVEL=3. Several major improvements in the newly developed LDD MOS device drain current model include: (1) a gate voltage and drain voltage dependent properties of the drain-source series resistance, (2) experimental determination of the saturation voltages, and (3) a very accurate subthreshold model.

A New Substrate Current Model

Based on the aforementioned effective electric field concept, an improved substrate current can be expressed as

$$\begin{aligned} I_B &= \frac{\alpha}{\beta \cdot l_d} I_D \cdot E_{eff} \cdot \exp(-\frac{\beta}{E_{eff}}) \\ &= \frac{\alpha}{\beta} I_D \cdot (V_{DS} - \eta V_{Dsat}) \cdot \exp(-\frac{\beta}{E_{eff}}) \end{aligned} \tag{2}$$

Here, $E_{eff}=(V_{DS}-\eta V_{DSAT})/l_d$ is the effective electric field within devices, which is bias dependent. l_d is the impact ionization length. V_{DSAT} is the saturation voltage which can be extracted from experimental data as illustrated in the previous section. The impact ionization coefficients adopt the values from [6], and are treated as fixed values in this study. Rearranging (2b), we can obtain another E_{eff} expression which gives

$$E_{eff} = \frac{V_{DS} - \eta V_{Dsat}}{l_d} = \frac{\beta}{\ln (\frac{I_D \alpha (V_{DS} - \eta V_{Dsat})}{I_D \beta}} \tag{3}$$

Here, I_D and I_B are the measured drain and substrate currents, respectively. l_d and η can be uniquely defined using extraction of (3). Fig. 6 shows the linear relationship between E_{eff} and V_{DS}. ηV_{Dsat} and l_d are found to be function of V_{GS}, as shown in Fig.7. Fig. 8 shows a verification of the modeled substrate currents with experimental data. Excellent match can be achieved for different channel lengths and bias conditions..

In summary, we add a new LDD MOS transistor substrate current model in Spice in addition to the drain current model. For the drain current characteristics, new features and enhancements of our previous model have been added for achieving accuracy and good convergency. For the substrate current, an accurate model and the associated parameter extractions is proposed based on the so called effective electric field, instead of the conventional peak electric field used by the lucky-electron (LE) concept. Comparison of the modeled results with those of experiment shows excellent match for a wide range of device channel lengths and bias conditions. The developed analytical model can be used for circuit level reliability simulation [3] in the current LDD MOS device technology.

Acknowledgements The financial support in part by the National Science Council under contract no. 81-0404-E009-620 is gratefully acknowledged.

References

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A. Strong Inversion Region

1. *Linear region* ($V_{GS} \geq V_T$ and $0 \leq V_{DS} < V_{DSAT}$)

$$I_D = \mu_n C_{ox}(W/L)[(V_{GS}-V_T)-0.5aV_{DS}]/ [(1+\theta(V_{GS}-V_T))(1+\eta V_{DS})+R_t(V_{DS}/V_{DSAT}) \beta_0(V_{GS}-V_T-0.5aV_{DS})] \quad \text{(A1)}$$

where

$$R_t = 0.5R_{V_{dsat}}/(V_{GS}-V_T-0.5aV_{DSAT})$$
$$R = R_0+R_1(V_{GS}-V_T)+R_2(V_{GS}-V_T)^2$$
$$\beta_0 = \mu_0 C_{ox}(W/L)/[1+\theta(V_{GS}-V_T)+\eta V_{DS}]$$
$$a = 1+0.5(K_1+K_3)g/\sqrt{\Phi_S-V_{BS}}-(K_2-K_4)$$
$$g = 1-1/[1.744+0.8364(\Phi_S-V_{BS})]$$

(2) *Saturation region* ($V_{GS} \geq V_T$ and $V_{DS} \geq V_{DSAT}$)

$$I_D = I_{d,sat}/(1-\delta L/L) \quad \text{(A2)}$$
$$V_{dsat} = (V_{GS}-V_T+aE_CL)/D-\sqrt{(V_{GS}-V_T+aE_CL)^2-2A(V_{GS}-V_T)E_CL/D}$$

where $D = a(1-\beta_0 RE_C)$

$V_{DSAT} = V_{dsat} + 2RI_{dast}$: terminal voltage

B. Weak Inversion Region

$$I_{sub} = (\mu_0 W/L)(\alpha C_{ox})(V_t)^2 e^{m[V_{GS}-V_T]}(1-e^{-V_{DS}/V_t}) \quad \text{(A3)}$$

where

$$m = m_0 f_1(L) f_2(W)(1+\lambda\sqrt{V_{SB}}) \quad \text{(A4)}$$

m_0 is the slope of a long channel device at zero back gate bias.

C. Transition Region

$$I_{D,W} = I_D + I_{sub}I_0/(I_{sub}+I_0) \quad \text{(A5)}$$

Table 1 Drain current model equations in the whole device operating regime.

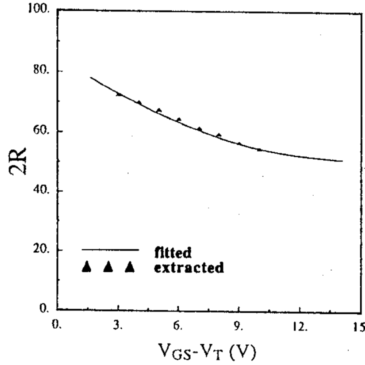

Fig. 2 The extracted drain-and-source series as functions of the gate voltages.

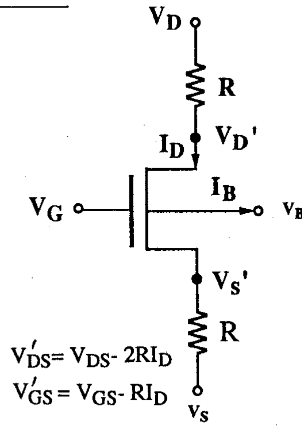

Fig. 1 The schematic diagram of an LDD MOS device.

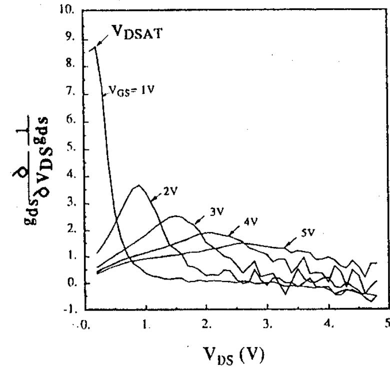

Fig. 3 Experimental determination of the saturation voltages, in which the peak values are the corresponding V_{DSAT} at each V_{GS}.

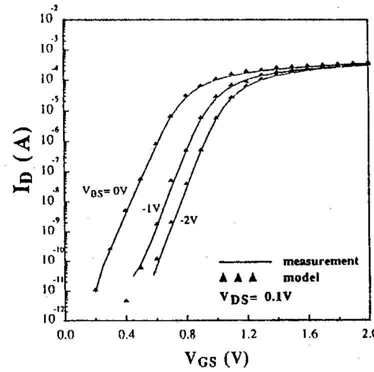

Fig. 5 Subthreshold characteristics of the same device in Fig.4.

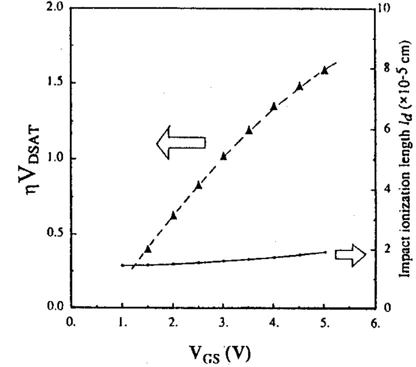

Fig. 7 Relationship between ηV_{Dsat}, l_d and V_{GS}.

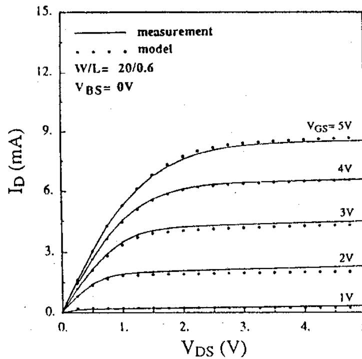

Fig. 4 Comparison of the experimental and modeled drain current characteristics of a short channel device.

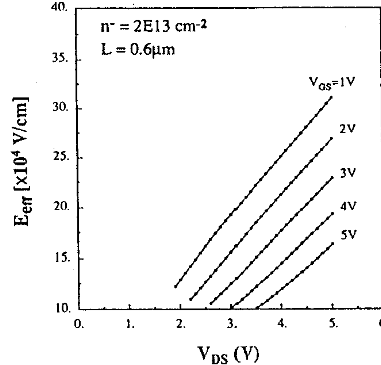

Fig. 6 Relationship between E_{eff} and V_{DS} for varous gate voltages.

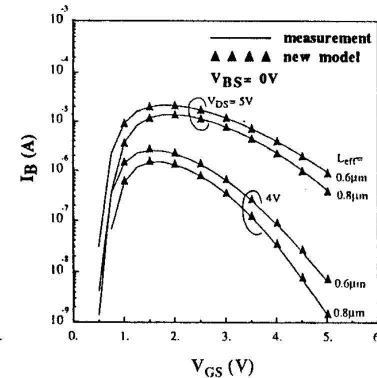

Fig. 8 Comparison of I_B between measured and modeled results for different channel lengths.