A New Semi-Empirical Model for
Amorphous Silicon Thin-Film-Transistors

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An accurate and efficient model for advanced Amorphous Silicon (a-Si:H) Thin-Film-Transistors (TFT) has been developed. This a-Si:H-TFT model accurately represents the second order effects which are important in advanced a-Si:H-TFT technology. The model makes it possible to get excellent agreement between measured and simulated data from the off region through the saturation region.

Presently, a-Si:H-TFTs are used widely for active matrix type Liquid-Crystal Displays (LCD). Some different physical theories and models which represented localized state behavior have been reported[1], [2]. These models, however, use a great number of exponential functions and are too slow and complicated to be used for LCD and other circuit simulations. A critical requirement of the model is to simulate off-screen noise of the LCD. Also, temperature and voltage stress effects, which are caused by back lighting of the LCD and applied voltage, must be implemented in the model. The characteristics of a-Si:H-TFT vary according to the device processing. The model, therefore, needs to be flexible for representing different types of a-Si:H-TFT devices.

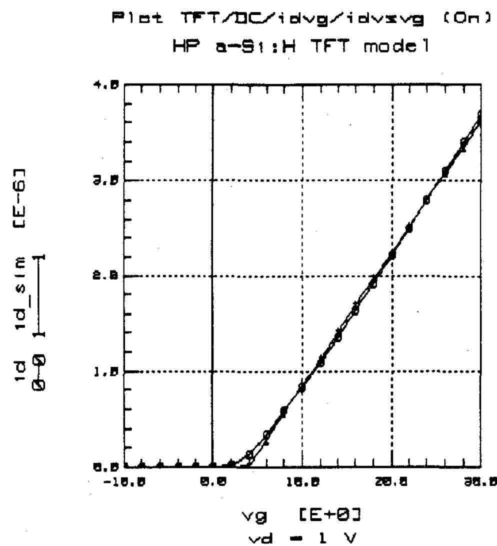
An advanced model has been developed to overcome the above limitations. In this model, the total gate charge is represented as the sum of localized charge, surface states charge, and mobile charge. The drain-to-source current at linear region is given by solving gradual channel approximation calculations. The localized states potential is represented as a static feedback of drain voltage.

$$Ids = \mu \cdot Cfm \cdot \frac{Weff}{Leff}\left((Vgs - Vth - \eta \cdot Vds)\, Vds - \frac{Vds^2}{2}\right)$$

The leakage current in the off-region that affects LCD noise simulation problems is modeled using simple algebraic equations. Temperature and voltage stress effects are modeled in a similar fashion. The model supports various thickness combinations of SiN_x and Ta_xO_y insulators in order to predict performance of advanced a-Si:H-TFT devices. Since a semi-empirical approach, such as that in the UCB MOS level 3 model, was used, the resulting model has fast simulation capability and flexibility. This model is currently being incorporated into the SPICE3 circuit simulator. A fully automated parameter extraction process has been developed for this model that calculates a full set of model parameters in less than 3 seconds. Typical RMS error resulting from this extraction is less than 5%.

This model has been tested on several a-Si:H-TFT processes. The attached figures are the sample data of a typical inverted stagger type a-Si:H-TFT. Excellent agreement between measured and simulated data has been achieved on all ranges of a-Si:H-TFT operation, including off-region leakage and saturation region.

As described above, this a-Si:H-TFT model has solved the major problems in simulating LCD structures, enabling designers to accurately simulate time domain characteristics and other important phenomena such as off-screen noise. The model represents a powerful tool for the design of large-area integrated circuits.



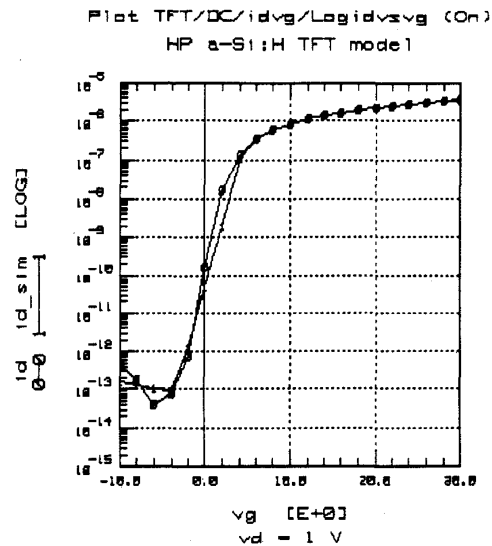


Figure 1. Ids vs. Vgs Plot

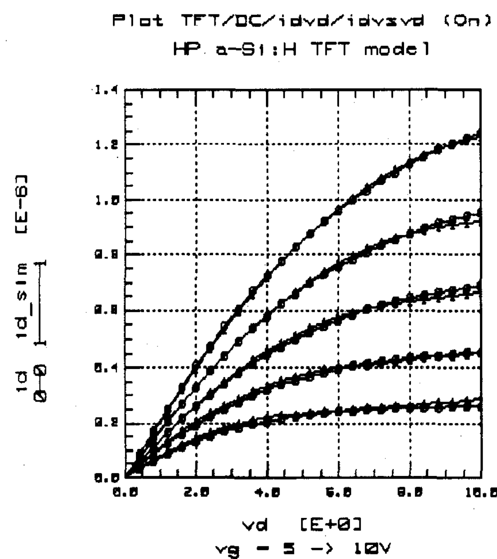


Figure 2. Ids vs. Vds Plot

Table 1: TFT Model Parameter List

Parameter	Definition
UO	Mobility
VTO	Zero voltage threshold voltage
NSS	Surface-state density
NFS	Fast surface state density
TSIN	Thin Si_xN_y thickness
TTAO	Thin Ta_xO_y thickness
PHI	Surface Potential
VMAX	Maximum drift velocity of carriers (Fitting parameter)
THETA	Mobility modulation
ETA	Static feedback on threshold voltage for Localized charge
GO	TFT leakage and or Optical fitting parameter
NU	First order temperature gradient (Empirical parameter)
CHI	Temperature exponential part (Empirical parameter)
PSI	Temperature exponential part (Empirical parameter)
K2	Temperature exponential part (Empirical parameter)
VTIME	Voltage stress
TREF	Temperature gradient of UO (Fitting parameter)
CGSO	TFT Gate to Source overlap capacitance
CGDO	TFT Gate to Drain overlap capacitance

References

[1] M. Shur et al., "A new model for amorphous silicon thin-film transistors", J. Appl. Phys. 66 (7), 1 October 1989
[2] K. Khakzar et al., "Model of Amorphous-Silicon Thin-Film Transistors for Circuit Simulators with SPICE", IEEE Trans. Electron Devices, vol. 39, no. 6, pp. 1428-1434, June 1992