Solid Modeling-Based Parametric Operations for Device Design

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Introduction

Parametric design of semiconductor devices and statistical exploration of how the device parameters impact device performance strongly depend on accurate and efficient device construction. This paper presents algorithms that take advantage of commercial solid modelling capabilities to explore guard ring spacing design rule variations for reducing substrate noise. Using the parametric structure algorithms and supporting methodology, multiple device structure variations were automatically created and smooth curves of substrate noise as a function of guard ring design rule spacing were generated.

Substrate Noise Analysis

Simulation experiments were conducted to examine substrate noise effects with guard ring spacing variations (parameter d in Figure 1) for two epitaxy thicknesses. The lumped element inductors connected to the guard ring and substrate contacts in Figure 1 model the package inductance. When clock noise is coupled capacitively to the lightly-doped epitaxy region on a heavily-doped substrate, the injected carriers travel to the analog circuit region via the heavily-doped substrate. To minimize this undesirable behavior, guard rings have traditionally been used for isolation. Figure 2 illustrates the impact that guard ring spacing and epitaxy thickness have on substrate noise. The graph values have been normalized to the substrate noise effect for an identical structure without a guard ring. As a result, for most values of d, the guard ring is not very effective in reducing the effect of substrate noise on the analog circuit.

Integrated System Flow

The parametric structure capability has been inserted in the Simulation Experiment Workbench, a rapid device prototyping environment [4]. Parameterized device structures are first graphically defined. Statistical design of experiment methodologies are then used to instantiate multiple devices. The system will automatically generate the mesh and device simulator input specification based on the structural and test specifications. Subsequently, device simulation will be executed concurrently through a distributed computing environment. Upon the completion of all simulations, data analysis modules are provided to enable users to extract desired design goal parameters and perform required analysis.

Algorithm for Parametric Operations

The parametric device design system requires more than the simple adoption of a conventional solid modeler. Many conceptual parametric transformations for device design cannot be directly mapped to conventional mechanical CAD boolean set operations. To bridge this gap, an encapsulation layer has been developed on top of a solid modeler to support the device parametric operations.

There are four types of parametric structure operations as shown in Figure 3 that are useful for device structure parameterization. A parametric dimension is used to model mask layout dimension variations as shown in Figure 3a. Parametric dimensions can also affect profile location and area (Figure 3b). A parametric thickness models etching and deposition effect variations (Figure 3c). A parametric angle is used to model angular changes (Figure 3d). The parametric attribute operation enables the variation of profile and boundary condition parameters (i.e., N_A, σ, work function, etc.).

Geometric parametric operations are further decomposed into simpler geometry operations called polygonal bounding region translation T(B, v) where B is a polygonal bounding region and v is the translation vector. It can be shown that an instance of a parameterized device can be obtained computationally by repeatedly applying bounding region translations provided that the basic bounding region translation can be implemented in the solid modeler. One such algorithm has been implemented for a boundary model-based geometry modeler ACIS [2] [3]. An outline of the algorithm is described in Figure 4 and Figure 5.

Conclusion

A set of parametric operations has been identified and implemented on a solid modeler to support manipulation and modification of the device structure. Device design space exploration is greatly facilitated with the ability to rapidly instantiate device structure variations. These structure variations were then used to analyze substrate noise behavior as a function of guard ring spacing and epitaxy thickness. A guard ring spacing design rule based on the tolerance to substrate noise could then be easily created.

Acknowledgments

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References

1. S. Tazawa, et al., IEDM Technical Digest, p. 173, 1992.
2. D. X. Yang and W. T. Wong, "Algorithms and Issues for Parametric Design," Technical Report, Stanford University, Stanford, CA, 1992.
3. Spatial Technology, Inc., "ACIS – Interface Guide," 1991.
4. W. T. Wong, J. Y-C. Pan, J. D. Plummer, "A Virtual Factory-Based Environment for Semiconductor Device Development," *Proc. IEEE ISMSS*, 1992.
5. M. Loinaz, D. Su, and B. A. Wooley, Symposium on VLSI Circuits, Digest of Tech. Papers, pp. 40-41, 1992.

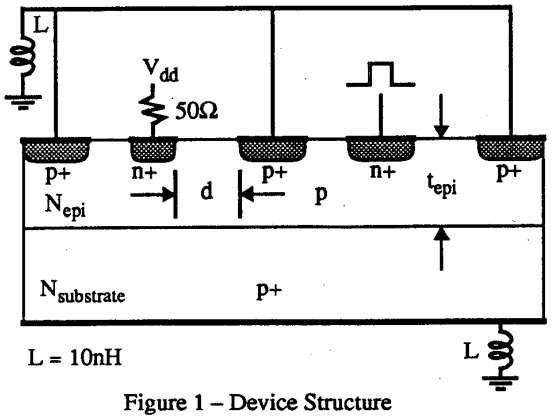

Figure 1 – Device Structure

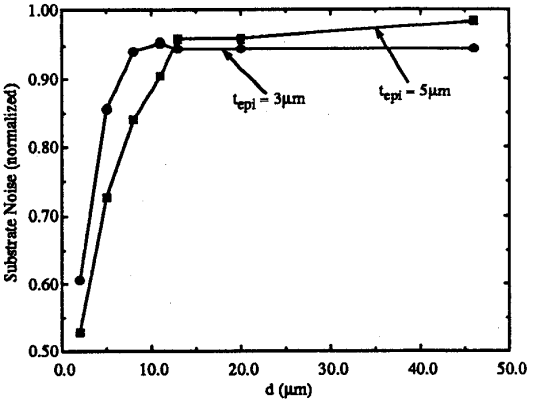

Figure 2 - Substrate Noise vs. Epitaxy Thickness and Guard Ring Distance

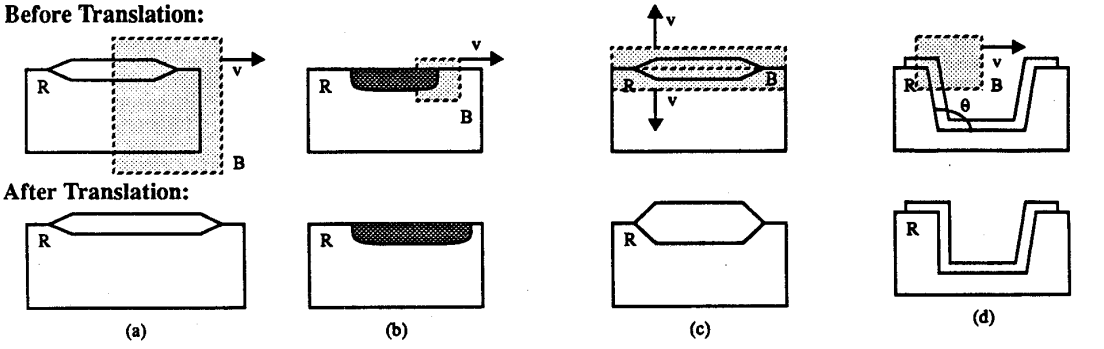

Figure 3 – Parametric Translation Operations

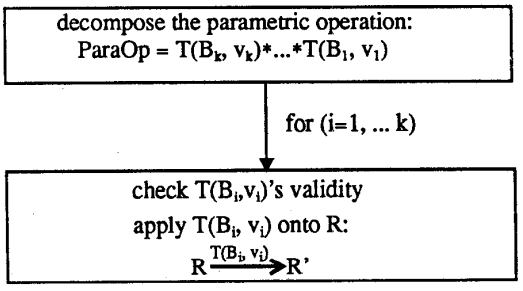

Figure 4 – Parametric Operation Algorithm

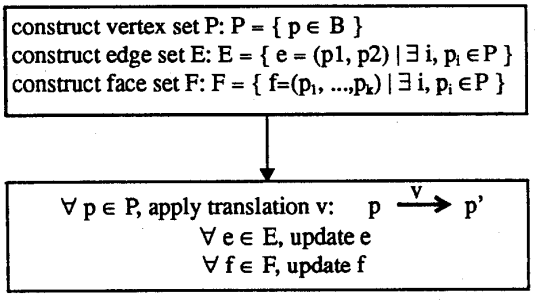

Figure 5 – T(B,v) Algorithm