A new consistent description of MOSFET performance for circuit simulation

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For circuit simulation a key issue is that all transistor characteristics such as DC currents as well as small signal conductances and capacitances can be described consistently on the charge storage Q in the transistor. In this sense existing analytical models are either valid only above the strong inversion or they don't include the short-channel effects in a consistent manner (see cf.[1]). We describe here a new analytical charge-sheet model which includes short-channel effects and describes all transistor characteristics for all regions/sizes/temperatures. A major benefit of the new model is its predictive capability over process generations and the small number of physical model parameters required.

Figure 1 presents charges calculated with our new model for a long-channel MOSFET as function of the gate voltage V_{gs}. A comparison between our model and 2D simulations carried out with GALENE is given in Fig. 2 for the long-channel case. Figure 3 shows a comparison of calculated Q_g values with the GALENE results for $L_{poly} = 0.6\mu m$. In this case the charge is shown as a function of V_{ds}, in addition each component of the total Q_g is included. For the short-channel case the contribution not only from the channel but also from the overlapped gate at the drain side is not negligible. This component is specified by "Drain" in Fig. 3. As seen from the figure this is the main origin of the V_{ds} dependence of Q_g.
Model parameter values are extracted from measured characteristics of drain currents I_{ds} as functions of applied voltages. The extracted parameter set gives universal results over many process generations due to the precise description of the extended charge-sheet model [2] and the globally characterized universal mobility model [3] employed, which also explicitly models charge modulated source/drain resistances. Figures 4 and 5 compare extraction of the low field mobility values μ_x for single process and global processes of universal mobility model as a function of $E_{eff}(= (Q_b + \eta Q_i)/\epsilon_{Si})$. The parameter η is about $\frac{1}{2}$ as usually derived, and Q_b and Q_i are the bulk and the intersion layer charge, respectively. Figure 6 shows calculated and measured I-V characteristics for the short-channel transistor.
Model development and validation resulted from extensive studies of not only terminal characteristics of which measurements are available but also internal stored charges Q. Consequences of the model consistency on circuit simulation results will be discussed by comparing with results for the conventional inconsistent model descriptions.

We show that all regions of transistor operation required for circuit simulation are accurately predicted. The physical nature of the model and its parameter efficiency directly attacks the remaining issues in circuit simulation: a) the complexity of the characterization over several process generations and b) the predictive requirements for statistical circuit design, based upon perturbation of a minimum set of physical model parameter values.

[1] Y. P. Tsividis, "Operation and modeling of the MOS transistor," McGraw-Hill, New York (1987).

[2] M. Mura-Mattausch and U. Weinert, IEICE Trans Electron., E75-C, p172-180 (1992).

[3] G. Yeric, A. Tasch and S. Banerjee, IEEE Trans. CAD, 9 (1990).

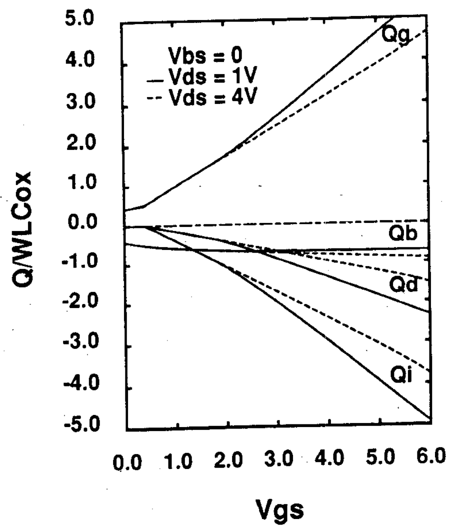

Fig.1. Calculated charges Q for $L_{poly} = 10\mu mm$.

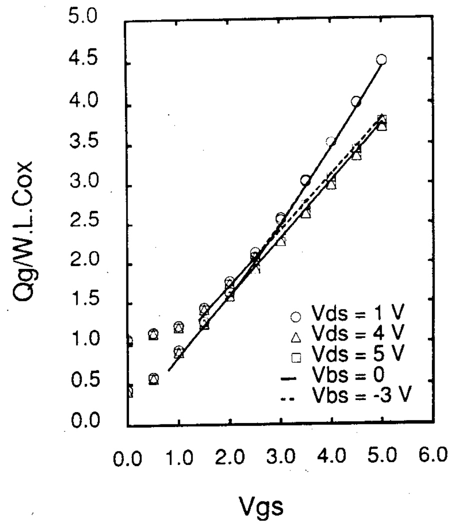

Fig.2. Comparison of Q_g with 2D simulation results by GALENE. Symbols are 2D results.

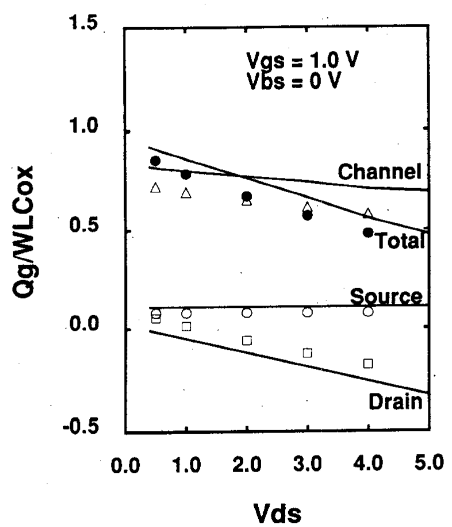

Fig.3. Comparison of calculated Q_g with 2D simulation results for $L_{poly} = 0.6\mu m$. Each component of Q_g is depicted as well.

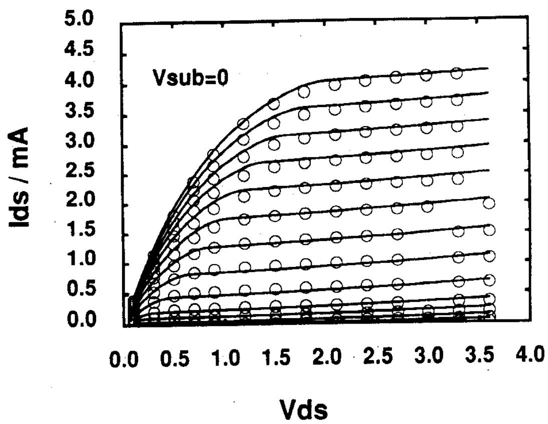

Fig.6. Calculated I_{ds} as a function V_{ds} for $L_{poly} = 0.6\mu m$. Open circles are measurements.

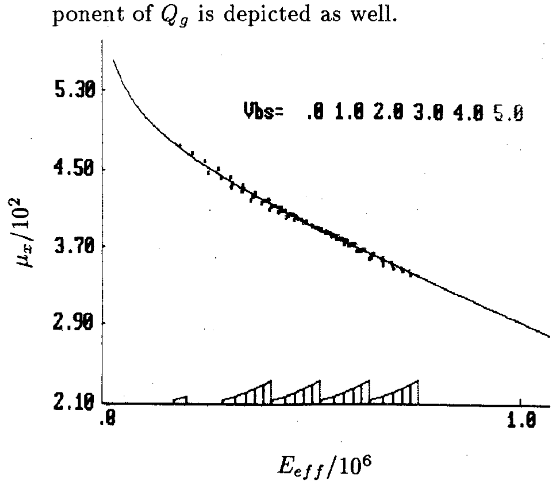

Fig.4. Extraction of low field mobility μ_x as a function of E_{eff} for single process.

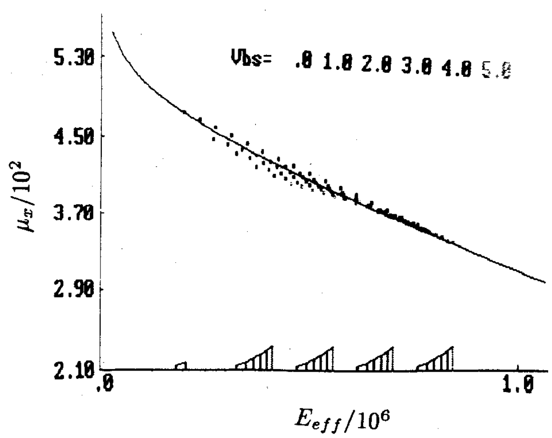

Fig.5. Same as Fig. 4 but for global processes.