An Analytical Delayed-Turn-on Model for Accumulation-Type Ultra-Thin SOI PMOS Devices Operating at $77K$

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Abstract

This paper presents a closed-form analytical delayed-turn-on model for accumulation-type ultra-thin SOI PMOS devices operating in the "delayed-turn-on" regime at liquid nitrogen temperature. As verified by the low-temperature PISCES results [1], the closed-form analytical delayed-turn-on model provides a good explanation of the delayed-turn-on behavior.

Summary

SOI MOS devices have been receiving lots of attention owing to its advantages in high speed and reduced second order effects [2]. Analysis of the SOI MOS device has been reported [3]-[6]. Cryogenic temperature performance o SOI MOS devices has also been reported [7]-[11]. However, most of them are inversion-type SOI MOS devices. Fo ultra-thin SOI structures, enhancement-type PMOS devices may be difficult to build using an n-type ultra-thin fil with an N+ polysilicon gate. Recently, an accumulation-type SOI PMOS device using a p-type ultra-thin film and an N+ polysilicon gate has been introduced to produce an enhancement-type PMOS device [12]. However, until now, lo temperature performance of the accumulation-type SOI PMOS device has not been reported. In this paper, analysi of the liquid nitrogen temperature performance of an accumulation-type SOI PMOS device is reported.

Fig. 1 shows the cross section of an accumulation-type ultra-thin SOI PMOS device structure [12] under study. The accumulation-type SOI PMOS device using an $N+$ polysilicon gate, has a front gate oxide of $200\mathring{A}$, a p-type thin silicon film of $1000\mathring{A}$ (t_{si}) and an insulator of $3500\mathring{A}$ (t_{ox2}). Three doping densities of the thin film – $1, 2, 4 \times 10^{16} cm^{-3}$ have been used. A p-type substrate with a doping density of $1 \times 10^{15} cm^{-3}$ has been assumed. In order to simplify the analysis, no interface charges have been assumed. Low-temperature PISCES [1] simulation has been used to obtain the results. As shown in Fig. 2, the operation of an accumulation-type SOI PMOS device working at $77K$ is partitioned into three regions - fully-turn-on, delayed-turn-on, and weak inversion. Between the fully-turn-on region and the weak inversion region, a unique "delayed-turn-on" region, which is similar to the delayed-turn-off phenomenon in the buried-channel PMOS device [13], can be identified.

Applying Poisson's equation in the thin film and accounting for incomplete ionization at $77K$ and using an "effective space charge density, in the region from the upper edge of the channel to the silicon surface, a closed-form analytica solution of potential at the top and bottom surfaces can be obtained. In the delayed-turn-on region, drain current is mainly diffusion current, which is exponentially proportional to the channel potential. Using a reference channel potential, ψ_{dto}, which is defined as the thin-film Fermi potential ($\psi_{dto} = -\phi_{fp}$), the IV characteristics at delayed turn-on can be expressed using the normalized inverse delayed-turn-on slope as shown in Eq. (1) in Fig. 3. In orde to evaluate the effectiveness of the analytical delayed-turn-on model for the accumulation-type SOI PMOS device the model results have been compared to the low temperature 2D PISCES results [1], where low temperature model have been included. Fig. 4 shows potential distributions in the center of the channel in the substrate direction in the accumulation-type SOI PMOS device with a thin film density of $1, 2, 4 \times 10^{16} cm^{-3}$, biased in the delayed-turn-on at $77K$ based on the analytical model and the PISCES results. A good agreement between the analytical model and the PISCES results can be found in the potential distribution.

Fig. 5 shows the subthreshold I-V characteristics of the PMOS device with three thin film densities ($1, 2, 4 \times 10^{16} cm^{-3}$) based on the analytical and PISCES results. For the case with a thin film doping concentration of $1 \times 10^{16} cm^{-3}$, delayed-turn-on phenomenon almost cannot be identified. For a higher thin film density, the PMOS device indicates a longer delayed-turn-on interval. In the delayed-turn-on region, the analytical model provides a very accurate prediction of the delayed-turn-on phenomenon in an accumulation-type SOI PMOS device operating at $77K$.

In the above analysis, no interface oxide charge atop the field oxide has been assumed. In fact, interface oxide charge may lead to a non-zero electric field ($E_f = \frac{Q_{ox2}}{\epsilon_{si}}$) at top of the field oxide in the thin film. This electric field is decreasing from the field oxide toward the front gate direction. As a result, the buried channel is not located at the field oxide any more. Instead, it's located at a zero electric field place, which is a distance of $\frac{Q_{ox2}}{qN_A}$ away from the field oxide in the thin film. Due to the existence of the non-zero electric field atop the field oxide, freezeout may vanish. Fig. 6 shows the interval of V_{GF} where delayed-turn-on exists vs. the doping density of the thin film the accumulation type SOI PMOS device without and with an interface oxide charge of ($2 \times 10^{11} cm^{-2}$) atop the field oxide operating at delayed-turn-on Generally speaking, for a higher doping density in the thin film, delayed-turn-on exists in a longer duration. With an oxide charge at the field oxide interface, delayed-turn-on lasts for a shorter period. Specifically, with an interface oxide charge of $2 \times 10^{11} cm^{-2}$, there is no delayed-turn-on if the doping density in the thin film is less than $2 \times 10^{16} cm^{-3}$.

References

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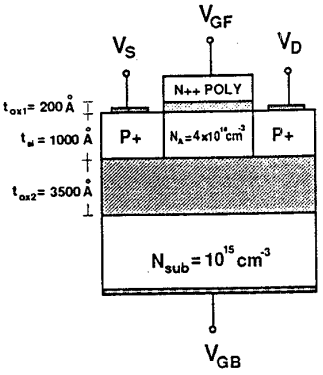

Fig. 1 The accumulation-type SOI PMOS device structure under study.

1. $n_{dto} = \frac{\partial V_{GF}}{\partial \psi_{s2}}|_{\psi_{s2}=\psi_{dto}} = \frac{(1+\frac{\sqrt{2q\epsilon_{si}}}{2C_{ox1}\theta_1}N_A)^{-1}\frac{\sqrt{2q\epsilon_{si}}}{2C_{ox1}\theta_1}(N_A-\theta_2)+\theta_3-\theta_4}{\theta_3-(1+\frac{\sqrt{2q\epsilon_{si}}}{2C_{ox1}\theta_1}N_A)^{-1}}$

$$U = \sqrt{N_A\frac{kT}{q} + n_p\frac{kT}{q}(e^{-1}-1)e^{-\psi_{s2}/\frac{kT}{q}} + N_A\frac{kT}{q}log\frac{1+Ke^{\frac{-(\psi_{s2}+\frac{kT}{q})}{\frac{kT}{q}}}}{1+Ke^{-\psi_{s2}/\frac{kT}{q}}}}$$

$$\frac{\partial x_c}{\partial \psi_{s2}} = \sqrt{\frac{\epsilon_{si}\frac{kT}{q}}{8q}}(e^{-1}-1)e^{-\psi_{s2}/\frac{kT}{q}}(n_p + \frac{N_AK}{(1+Ke^{\frac{-(\psi_{s2}+\frac{kT}{q})}{\frac{kT}{q}}})(1+Ke^{-\psi_{s2}/\frac{kT}{q}})})/U^3$$

$$\theta_1 = \sqrt{N_A(\psi_{s1}-\psi_{s2}) - n_p\frac{kT}{q}e^{-\psi_{s2}/\frac{kT}{q}} - N_A\frac{kT}{q}log(1+Ke^{-\psi_{s2}/\frac{kT}{q}})}$$

$$\theta_2 = (n_p + \frac{N_AK}{1+Ke^{-\psi_{s2}/\frac{kT}{q}}})e^{-\psi_{s2}/\frac{kT}{q}}$$

$$\theta_3 = \frac{(t_{si}-x_c)}{(t_{si}-x_c)+\frac{2\epsilon_{si}}{C_{ox1}}}$$

$$\theta_4 = 1 + \frac{(\psi_{GF}+\frac{Q_{ox1}}{C_{ox1}}-\frac{kT}{q}-\psi_{s2})}{(t_{si}-x_c)+\frac{2\epsilon_{si}}{C_{ox1}}}(\frac{(t_{si}-x_c)}{(t_{si}-x_c)+\frac{2\epsilon_{si}}{C_{ox1}}} - 1)\frac{\partial x_c}{\partial \psi_{s2}}$$

$$x_c \equiv \frac{kT/q}{E(\psi(x)=\psi_{s2}+\frac{kT}{q})}$$

Fig. 3 Important equations.

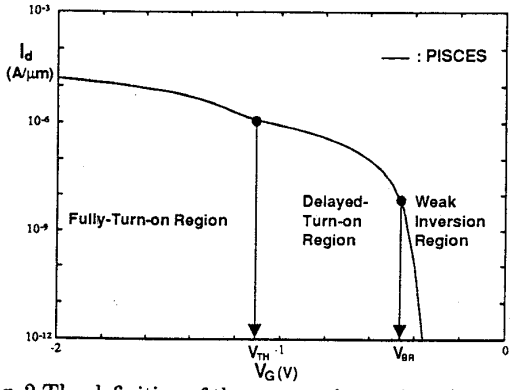

Fig. 2 The definition of three operation regions (strong inversion, delayed-turn-on, weak inversion), of an accumulation-type SOI PMOS device at $77K$.

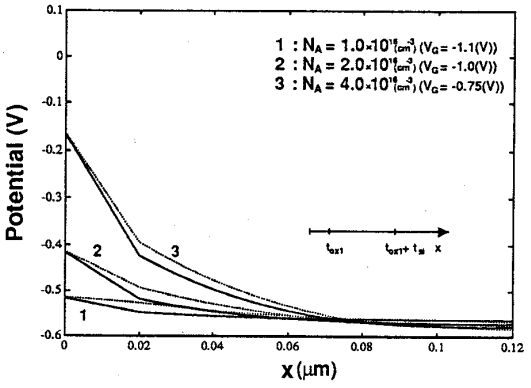

Fig. 4 Potential distributions in the center of the channel in the substrate direction in the accumulation-type SOI PMOS device with a thin film density of $1, 2, 4 \times 10^{16} cm^{-3}$ biased in the delayed-turn-on at 77K based on the analytical model and the PISCES results.

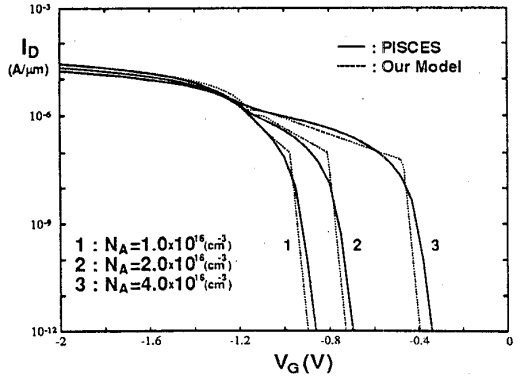

Fig. 5 The I_D vs. V_{GS} characteristics of the accumulation-type SOI PMOS device operating at $77K$ using the analytical model and the PISCES results.

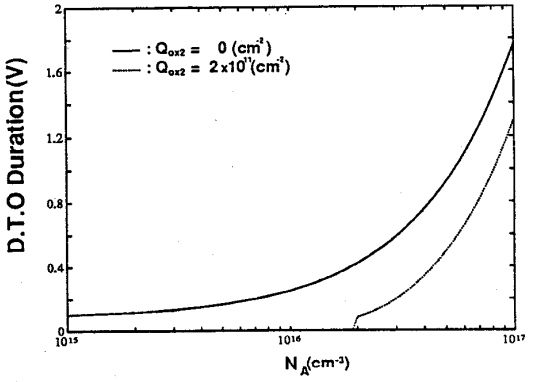

Fig. 6 The voltage interval where delayed-turn-on exists vs. the thin film doping density of the accumulation-type SOI PMOS device with and without an interface oxide charge of $2 \times 10^{11} cm^{-2}$ atop the field oxide, operating at $77K$.