Characterization of Metallurgical Channel Length and Gate Electrode's Physical Dimension for Device Analysis and Calibration of Numerical Process and Device Simulators

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Accurate determination of metallurgical channel length (L_{met}), and gate electrode's physical dimension (L_{gate}) and fringing capacitance (C_{fr}) of submicron MOSFETs is of fundamental value to the study of cause-effect relation between processing condition and device's performance and reliability, device scaling, and the calibration of physical models in numerical process and device simulators. Comparing to conventional methods [1-4], this paper describes two capacitance-based measurement techniques for non-destructive and much more accurate characterization of L_{met}, L_{gate} and C_{fr}, while requiring only simple device structures. L_{met} characterization is based on the independence of MOSFET's gate-source/drain capacitance (C_{gs}) on gate bias (V_{gs}) at V_{gs} up to the channel inversion threshold (V_{gs}^{on}) and the assumption that L_{met} can be determined from C_{gs}^{on}, the capacitance at V_{gs}^{on}. On the other hand, the determination of L_{gate} utilizes the V_{gs} dependence of MOS capacitor and the linear dependence of MOS capacitance on L_{gate}. A fundamental assumption in L_{gate} extraction is the V_{gs} independence of C_{fr}. Simulation of a wide range of MOSFET and MOS capacitor structures that are different in gate oxide thickness (T_{ox}), LDD and channel doping concentration, and source/drain reoxidation induced T_{ox} thickening have been performed to understand and evaluate in detail the various assumptions, and the applicability and limitations of these two device characterization techniques. The results demonstrated consistently that the accuracy in L_{met} and L_{gate} extraction from capacitances is better than 150 Å. The device characterization techniques presented in this paper have been applied to MOSFET and MOS capacitors fabricated in several submicron CMOS technologies.

Extensive numerical device simulation have shown that L_{met} of submicron MOSFETs determined from $[C_{gs}(V_{gs}^{inv}) - C_{gs}^{on}]/C_{ox}$ agree with values obtained directly from channel doping profiles to within 150 Å (Fig. 1). $C_{gs}(V_{gs}^{inv})$ and C_{ox} are, respectively, the total gate capacitance of short channel MOSFETs and the per unit area gate capacitance of large area capacitor at very high inversion levels. Detailed numerical results have also demonstrated the applicability of this technique to MOSFETs with T_{ox} ranging from 40 to 150 Å, wide range of LDD impurity profiles (Fig. 2), non-uniform T_{ox} due to source/drain reoxidation (Fig. 3) and poly gate depletion. The physical reason for achieving highly accurate extraction even in the presence of fringing field between the source/drain side wall and the gate was investigated using device simulation (Fig. 4). The cause for degradation in L_{met} extraction accuracy when $T_{ox} > 200$ Å was also studied. Noted that the data selection for and the accuracy of L_{met} determination is well-defined and is better than 150 Å as compared to 0.1 μm for the methods discussed in [2-4]. This method has been applied to characterize L_{met} of fabricated n- and p-channel MOSFETs (Fig. 5). Extensive experimental data demonstrated the repeatability in data acquisition and the consistency in L_{met} extraction. In addition, the electrical channel length (L_{eff}) extracted from drain current and L_{met} from capacitance data are compared to demonstrate the incorrectness in using L_{eff} as a quantitative measure of submicron MOSFET's metallurgical channel length (Fig. 6).

Detailed device simulation was used to validate the physical basis of the L_{gate} characterization method including the bias independence of C_{fr}, the proximity effect of the heavily doped regions resulted from poly gate implant in self-aligned CMOS technologies, limits of its applicability in terms of channel doping concentration and T_{ox}, and the consistency in extracted L_{gate} using data at different biases. The theoretical analysis of the L_{gate} characterization method has been partially presented in [5]. In this paper, experimental CV data and experimental verification of the accuracy in L_{gate} extraction will be presented for the first time.

Combined experimental results from L_{met} and L_{gate} characterization have been applied to calibrate model parameters in device and process simulators for modeling physical effects such as velocity saturation, punchthrough, threshold voltage variation with L_{eff}, and 2-D impurity diffusion.

References

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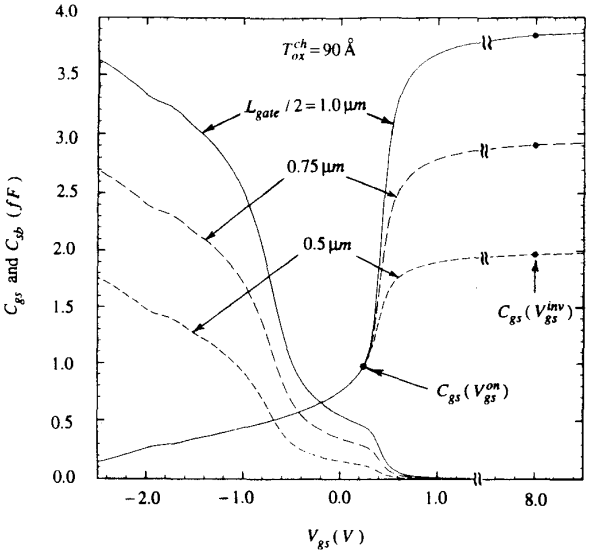

Fig. 1

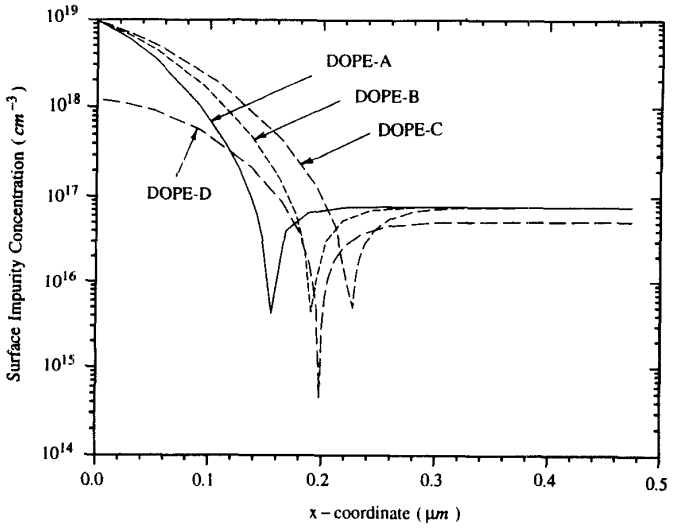

Fig. 2

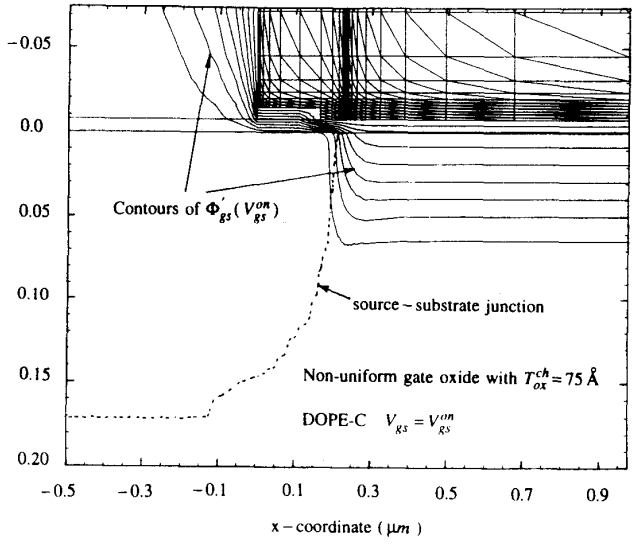

Fig. 3

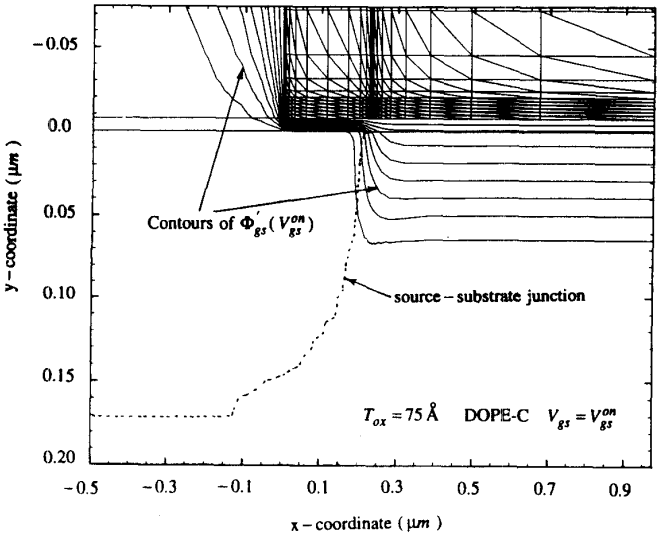

Fig. 4

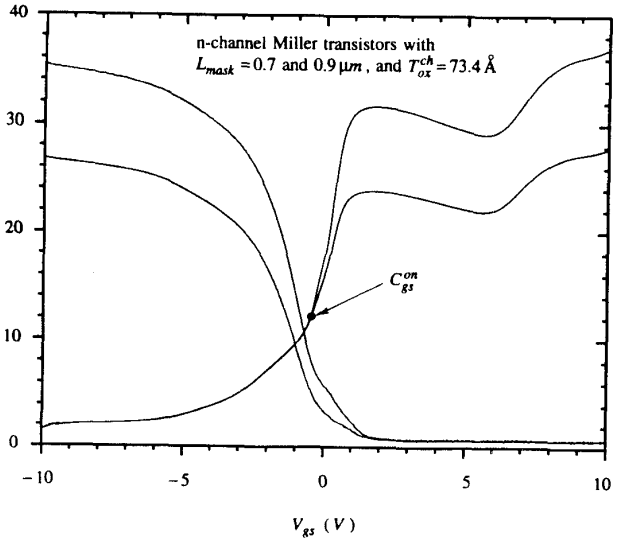

Fig. 5

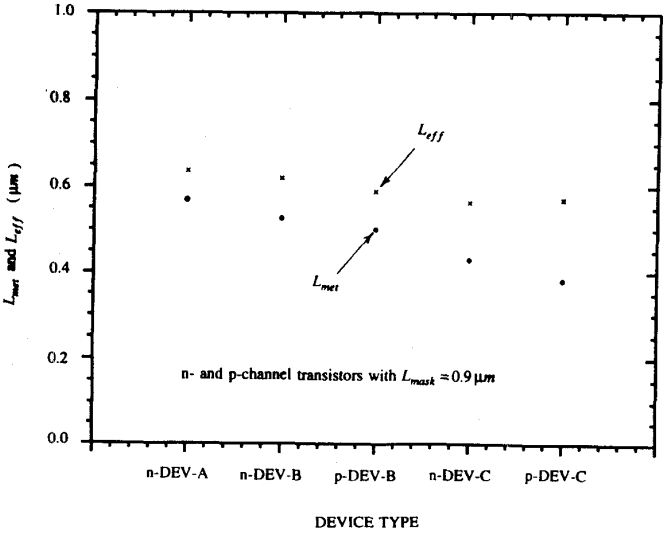

Fig. 6