Monte Carlo analysis of hot carrier effects in ultra small geometry MOSFETs

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INTRODUCTION

Fabrication of MOSFET with channel length down to $0.1\mu m$ has been recently achieved [1,2]. This work intends to provide an investigation on hot carrier effects for extremely short devices. In particular, the gate length (L_G) dependence of carrier heating is studied. This is a topic of great interest as recent experimental works carried out on n-MOSFETs gave opposite results reporting a decreasing substrate current for $L < 0.15\mu m$ [1] or an always increasing I_{sub} for decreasing L [2].

The semi-classical model for electron transport in silicon (i.e. the Boltzmann transport equation) is adopted. Quantum effects due to reduced device dimensions and high electric fields are not included but, in spite of that, we consider this simple framework adequate in order to obtain a qualitatively correct scenario. Simulations have been performed by a self-consistent Monte Carlo simulator [3,4] for devices with L_G between $0.15\mu m$ and $0.025\mu m$. Two different device structures are considered. The first one features a thin (10 nm) undoped epitaxial layer grown over an highly doped substrate, a thin oxide thickness (3 nm) and ultra shallow LDD type source and drain ($x_j = 10nm$) (Fig.1,a) ; by drift diffusion analysis, this structure proved to be scalable down to $L_G = 0.05\mu m$ adopting $V_{DD} = 1.2V$ without showing particularly critical short channel effects (S factor lower than 90). The second structure (Fig. 1,b) is a modification of the SOI MOSFET featuring a back oxide thickness equal to that of the front gate oxide (double gate MOSFET [5]). In our simulations the silicon layer thickness was 10 nm and the oxide thickness was 3 nm for both the front and the back insulators; source and drain feature the same characteristics of the epi case. This structure presents very good short channel effects for $L_G = 0.025\mu m$ and $V_{DD} = 1.2V$.

SIMULATION RESULTS

Figs. 2,3 report the electric field profile and the electron mean energy (ϵ) computed by MC simulation of the epi devices with $L_G = 0.15, 0.05, 0.025\mu m$ biased with $V_{DS} = 2.5V$, $V_{GS} = 1.25V$; in order to have a fare comparison, the gate work function for the devices was modified to obtain the same threshold ($0.3V$) independently of channel length and device structure. Reducing the gate length from 0.15 to $0.05\mu m$ does not appreciably affect the maximum electric field but leads to an increase of the channel field (i.e. the electric field in the channel region between the source and the pinch-off point) in qualitative agreement with the results of [2]. The maximum value of the electron mean energy ($< \epsilon >_{max}$) is correspondingly increased by more than 10%. For $L_G = 0.025\mu m$ it is not possible to distinguish a channel region and a pinch-off region; in spite of a relevant increase of the maximum electric field, a little variation of the mean energy peak value is obtained. This latter effect may be attributed to the increase of the abruptness of the electric field profile at decreasing L_G that causes relevant non-local effects. Electron energy needs a finite time to reach equilibrium with the local field and the delay of the carrier heating process increases for steeper field profiles.

The results above are confirmed by the calculated values for the ratio I_{sub}/I_{ds} reported by Fig. 4. Such ratio, usually considered a good monitor of hot carrier in MOSFETs, sligthly increases for L_G down to $0.025\mu m$ in qualitative agreement with the experimental results in [2]

In the case of the double gate structure, an even weaker carrier heating dependence on on L_G is found, also due to the lower gate length dependence of the electric field peak value (Figs. 5,6). The mean energy peak value is almost independent of L_G in the considered range (Fig. 5) while a weakly increasing I_{sub}/I_{ds} (Fig. 4) for decreasing L_G is mainly due to the fact that in the shortest devices a larger portion of the whole channel presents significant heating.

An interesting proof of the importance of non-local effects can be obtained by comparing the two structures at the same gate length. Let us consider $L_G = 0.5\mu m$: in the case of the DG structure, in spite of an higher electric field peak value (Figs. 2,5), a lower $< \epsilon >_{max}$ is attained than in the epi case. This is due to a much more abrupt electric field profile resulting in a lower field in the channel region before the pinch-off point and leading to more pronounced non-local effects on carrier heating.

CONCLUSIONS

The results of this work prove that scaling of devices to $L_G < 0.1\mu m$ will not cause dramatic increase of hot carrier effects even without scaling the V_{DD} value. Furthermore, it is shown that in the case of very short devices, hot carrier analysis based on maximum electric field are not only of little significance, but may lead to erroneous conclusions.

REFERENCES

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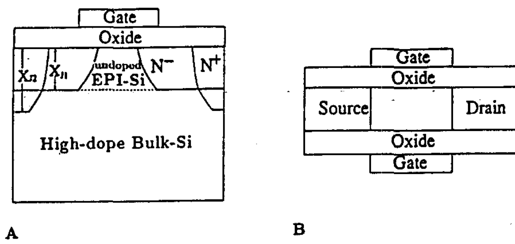

Fig. 1 n-MOS structures ;A): Epi MOS; B): Double gate MOS

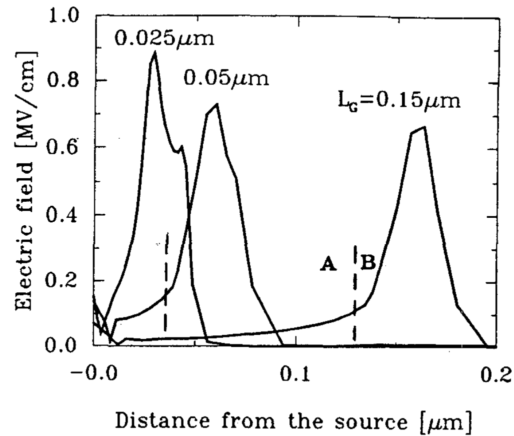

Fig. 2 : Electric field at the interface of epi-MOSFETs ($L_G = 0.15, 0.05, 0.025\mu m$; $V_{DS} = 2.5V, V_{GS} = 1.25$) Dashed lines : transition between channel (A) and pinch-off region (B).

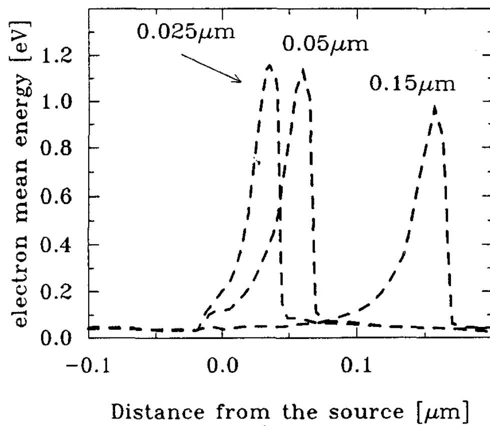

Fig. 3 : Electron mean energy along the interface of epi-MOSFETs ($L_G = 0.15, 0.05, 0.025\mu m$; $V_{DS} = 2.5V, V_{GS} = 1.25$).

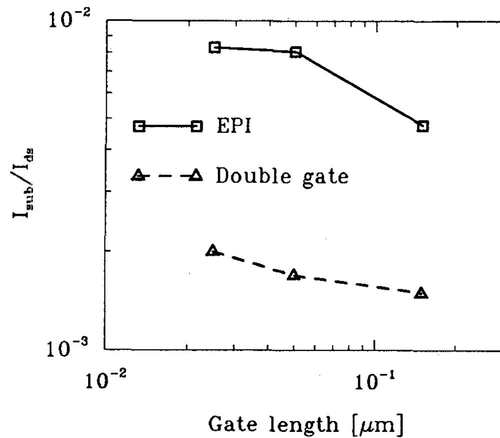

Fig. 4: I_{sub}/I_{ds} as a function of gate length for epi- and double gate MOSFETs. $V_{DS} = 2.5V, V_{GS} = 1.25$.

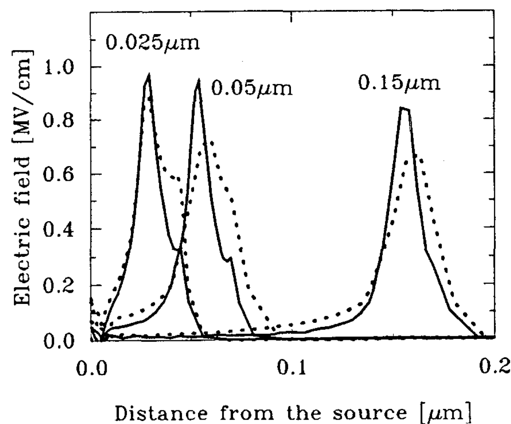

Fig. 5 : Electric field along the interface of double gate MOSFETs ($L_G = 0.15, 0.05, 0.025\mu m$; $V_{DS} = 2.5V, V_{GS} = 1.25$). Dotted lines are the corresponding results for the epi devices.

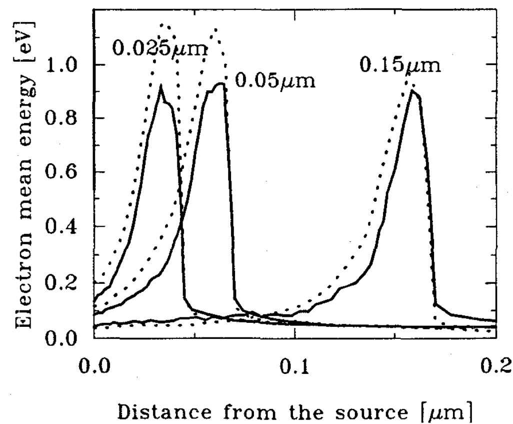

Fig. 6 : Electron mean energy at the interface of double gate MOSFETs ($L_G = 0.15, 0.05, 0.025\mu m$; $V_{DS} = 2.5V, V_{GS} = 1.25$). Dotted lines are the corresponding results for the epi devices.