Two-Dimensional Simulation of GaAs MESFETs Including Impact Ionization of Carriers and Carrier Trapping in the Semi-insulating Substrate

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To understand the drain-to-source breakdown mechanism in GaAs MESFETs is important for realizing high-performance GaAs LSIs, but it has not been well clarified. Recently, an abrupt increase in output conductance with the drain voltage ("kink") is often reported experimentally, and sidegating effects become remarkable in this kink region[1]. This suggests that when interpreting the kink or the breakdown, effects of carrier trapping in the semi-insulating substrate should be considered. Some theoretical works on the breakdown have been made and one of them simulates I-V curves by considering impact ionization[2], but it neglects carrier trapping by deep levels in the substrate. So, in this work, we have mode 2-D simulation of GaAs MESFETs in which impact ionization of carriers and deep levels in the semi-insulating substrate are considered, and have found that the "kink" is explained by impact ionization of carriers and the following carrier trapping in the substrate.

A device structure simulated here is shown in Fig.1. We consider two types of substrates: (a) undoped semi-insulating LEC GaAs where deep donors "EL2" (N_{EL2}) compensate shallow acceptors (N_{Ai}), and (b) Cr-doped semi-insulating GaAs where deep acceptors "Cr" (N_{Cr}) compensate shallow donors (N_{Di}). Usually, EL2 acts as an electron trap, while Cr acts as a hole trap[3]. Basic equations are the Poisson's equation and continuity equations for electrons and holes that include carrier generation rate by impact ionization. We have studied dependences of calculated I-V curves on the substrate type and on the trap densities in the semi-insulating substrate. The following features are pointed out.

(1) In a case with high Cr density in the substrate ($N_{Cr}= 10^{16}cm^{-3}$), a kink due to impact ionization is observed at low voltage region ($\sim$ 1.5 V), as shown in Fig.2 (No kink is observed for a case with undoped substrate in this region). Holes are generated at the drain edge of the gate due to impact ionization and flow into the substrate. These holes are captured by hole traps Cr (deep acceptor), and the ionized Cr density decreases as shown in Fig.3. So, the channel thickness increases and hence the "kink" arises. It is interpreted that in a case with EL2 (electron trap), the change of ionized EL2 density by capturing holes is relatively small ($< 10^{12}$ cm^{-3}) in this voltage region, and hence the kink is not observed.

(2) In cases with low acceptor densities ($< 10^{14}cm^{-3}$) in the substrate, as shown in Fig.4, other type of kink due to impact ionization is observed at relatively high voltage region ($\sim$ 15 V). Hole densities in the substrate become much higher than the acceptor density (Fig.5) and modulate electron densities directly. In this case, the kink occurs due to so-called "conductivity modulation" in the substrate.

(3) In a case with high acceptor density in the undoped semi-insulating substrate ($N_{Ai}= 10^{16}cm^{-3}$), I-V curves show complicated features in the relatively high voltage region, as shown in Fig.6. Two kinks are observed at V_D= 3 $\sim$ 5 V and at V_D= 10 $\sim$ 15 V. By studying carrier density, ionized-trap density, and potential profiles, we interprete that the former kink arises because holes generated by impact ionization are captured by EL2 (deep donor) and the positive charge density in the substrate is increased much to affect the channel thickness. The latter kink arises because the hole density becomes high enough to dominate the space-charge distribution in the substrate and hence the channel is widened. In these voltage regions, EL2 acts as a recombination center and not as an electron trap.

It is concluded that carrier trapping effects in the semi-insulating substrate are important and have to be taken into account when interpreting kink effects and/or breakdown phenomena in GaAs MESFETs.

[1] A.Harrison, IEEE Electron Device Lett., Vol.13, pp.381-383, 1992.
[2] Y.Wada and M.Tomizawa, IEEE Trans. Electron Devices, Vol.35, pp.1765-1770, 1988.
[3] K.Horio, Y.Fuseya, H.Kusuki and H.Yanai, IEEE Trans. Computer-Aided Design, Vol.10, pp.1295-1302, 1991.

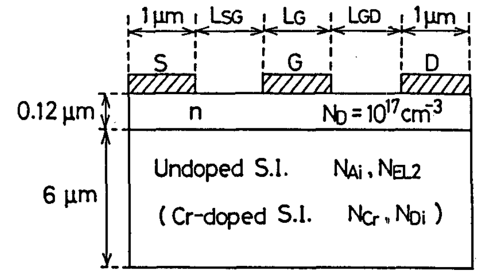

Fig.1 Device structure simulated here. L_G is typically 0.3 μm. L_{SG} and L_{GD} are both set to 1.35 μm in this study.

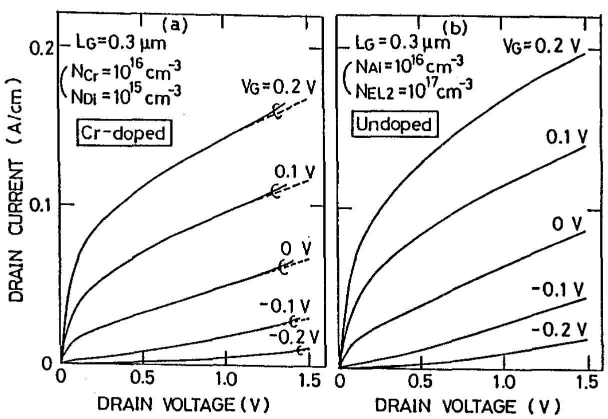

Fig.2 Calculated drain characteristics of GaAs MESFETs on (a)Cr-doped and (b)undoped semi-insulating substrates. $N_{Cr}= N_{Ai}= 10^{16} cm^{-3}$.
(—): With impact ionization
(---): Without impact ionization

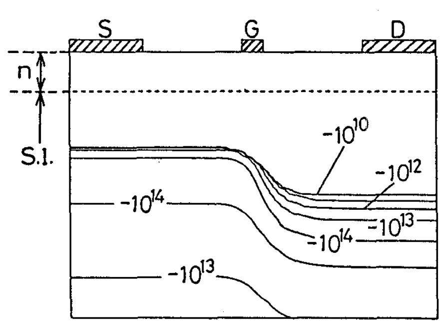

Fig.3 Difference of ionized Cr density ΔN_{Cr}^- between the two cases (with and without impact ionization), corresponding to Fig.2. V_G = 0 V and V_D = 1.3 V.

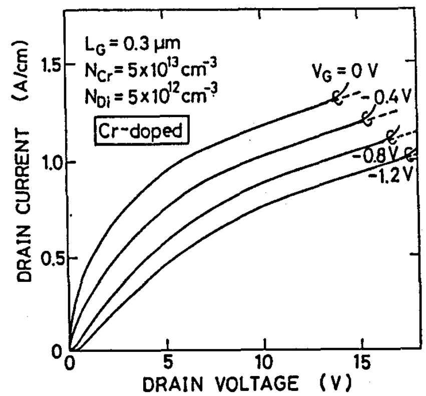

Fig.4 Calculated drain characteristics of GaAs MESFETs on Cr-doped semi-insulating substrate with low N_{Cr} of $5x10^{13} cm^{-3}$.
(—): With impact ionization
(---): Without impact ionization

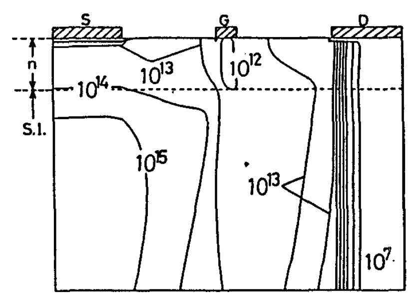

Fig.5 Hole density profiles of GaAs MESFETs on Cr-doped semi-insulating substrate (N_{Cr}= $5x10^{13} cm^{-3}$). V_G = 0 V and V_D = 14.25 V.

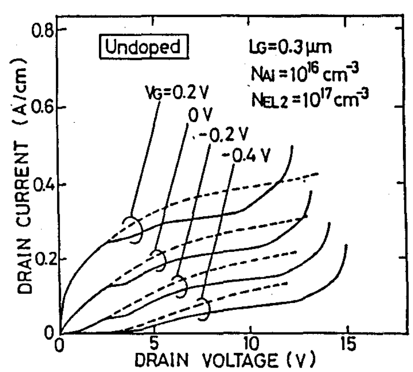

Fig.6 Calculated drain characteristics of GaAs MESFETs on undoped semi-insulating substrate with high N_{Ai} of $10^{16} cm^{-3}$.
(—): With impact ionization
(---): Without impact ionization