Analysis of Collector Signal Delay in Bipolar Devices using a Monte Carlo Method

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In high-speed bipolar junction transistors(BJTs), the high doping levels applied to the base and collector cause degradation of the junction breakdown voltage. It has been suggested[1] that insertion of a lightly doped (intrinsic) layer (an i-layer) might reduce the electric field within the base-collector depletion region of BJTs, and thus increases the breakdown voltage. There is a possibilty, however, that such profile modifications may affect high-speed performance, since the reduced field may also reduce the carrier velocity in the depletion region. Within the regime where the drift diffusion model of electron transport applies, this i-layer may cause few problems because velocity saturations are easily achieved with relatively weak ($\sim 10^4 V/cm$) electric fields. However, when device dimensions are scaled down to the size where non-stationary effects, such as velocity overshoot, can no longer be ignored, determining to what extent the above has an effect becomes a non-trivial question.

It has also been pointed out[2] that when the carrier velocity is not uniform throughout the BC depletion region, the collector signal delay τ'_{bc} is not given by the conventional formula $\tau'_{bc} = \tau_{bc}/2$ where τ_{bc} is the collector transit time, but by the expression

$$\tau'_{bc} = \int_0^W \frac{dx}{v(x)}\left(1 - \frac{x}{W}\right) \tag{1}$$

where W is the depletion region width and $v(x)$ is the carrier velocity function in this region. Thus the overall collector signal delay is determined by the contributions of two competing factors, $1/v(x)$ and $1 - x/W$.

In this work we analyze using a Monte Carlo method the effects of velocity overshoot on collector signal delay, both with and without an i-layer. For this purpose, we adopt a simple model of a bipolar device, as depicted in Figs.1 and 2, with i- or n^--layers inserted between the base and collector buried n^+-layers.

Prior to the MC calculations, a drift diffusion(DD) simulation using MOS2C[3] was performed and the bias conditions just prior to entering the high-injection region were isolated. Figs. 3 show the electric field distributions in the devices. The i-layer causes the reduction of maximum field in the depletion region, about 50 % for $W_c = 0.1(\mu m)$ case and 30 % for $W_c = 0.05(\mu m)$ case, respectively. In Figure 4, the DD results for electron velocity distribution in the device with $W_c = 0.05(\mu m)$ are presented. It is clear that velocity saturation at $1.1 \times 10^7 (cm/s)$ occurs throughout the depletion region in both i- and n^-- cases. Thus the DD simulation indicates that there is no essential difference between these cases.

Next, the Monte Carlo simulation was carried out for these devices using BEBOP[4]. The calculated electron velocities are summarized in Figs.5(a) and (b). In contrast to the DD results, strong velocity overshoot was observed at the BC junction. As clearly seen from (1), this characteristic is advantageous as regards collector signal delay. Inspection of the figures reveals that the maximum velocity is greater in the n^-- case for both values of W_c, although the margin is smaller when $W_c = 0.05(\mu m)$. On the other hand, it should be noted that the velocity is greater in i-layer cases deep inside the region. This can be attributted to the greater suppression of impurity scattering in i-layers than in n^--layers.

Figure 6 gives the estimated collector transit times and collector signal delays obtained using equation (1). In devices with $W_c = 0.1(\mu m)$, the collector transit times are almost the same for both i- and n^-- cases($\simeq 1.35(ps)$), but the signal delays are estimated to be $0.37(ps)$ and $0.26(ps)$, respectively. In this case the effect of maximum velocity near the BC junction seems to be dominant. When W_c is made smaller, however, the disadvantage of the i-layer tends to be less pronounced. In devices with $W_c = 0.05(\mu m)$ the transit times are $0.60(ps)$ for the n^--layer case, and the signal delays are estimated to be $0.13(ps)$ for the i- case, $0.14(ps)$ for the n^-- case. Care must be taken that these small differences are not taken too seriously at present, since they are beyond the resolution of our calculations, and conclusion should be that there were no significant differences. In this case the greater velocity deep inside the depletion region compensates the smaller maximum velocity of the i-layer case.

Finally, we give a brief discussion on the electron mean energy which is closely related to I/I rate and breakdown voltages. Figs.7(a) and (b) show the electron mean energy distributions in the devices. When $W_c = 0.1(\mu m)$, we find in the i-layer case considerable suppression of the peak value which may lead to substantial increase in the breakdown voltage, whereas no essential difference between n^-- and i-layer cases is observed when $W_c = 0.05(\mu m)$. It is likely that no improvement in the breakdown voltage is achieved in this device despite the 30% reduction of the maximum electric field.

In conclusion, by applying a MC simulation to bipolar transistors, the effects of i-layers on collector signal delay–which cannot be detected by DD simulation–was clarified. When the i-layer thickness is $0.1(\mu m)$, reduction in the speed performance was observed. When the thickness is $0.05(\mu m)$ the performance is recovered through velocity overshoot which is completely different mechanism from the DD model, perhaps with no advantage in breakdown voltages.

References

[1] D.D.Tang and P.-F.Lu, *IEEE EDL* **10**, 67(1989)
[2] S.E.Laux and W.Lee, *IEEE EDL* **11**, 174(1990)
[3] T.Kobori and T.Wada, *IEICE Trans.* **E74**, 1634(1991)
[4] Venturi *et al*, *IEEE TCAD* **10**, 1276(1991)

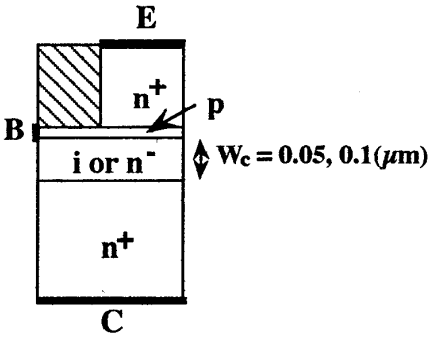

Fig. 1 Structure of the Bipolar device used in the simulation. Thick lines represent the electric contact.

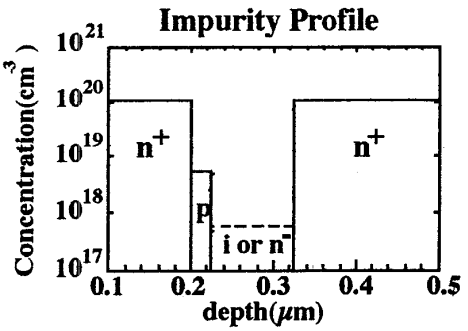

Fig. 2 Doping profile of the device. Concentration of the i- and n^- layers are $10^{14}(cm^{-3})$ and $5 \times 10^{17}(cm^{-3})$, respectively.

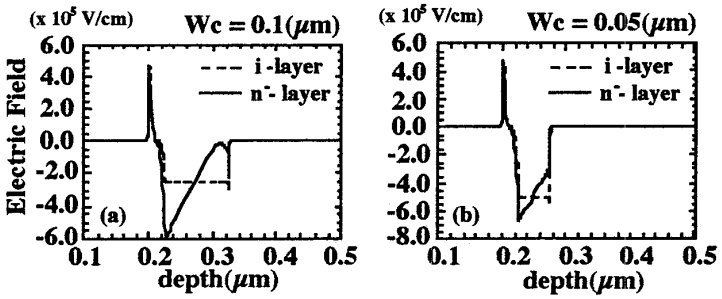

Fig. 3 Electric Field distributions at $V_{ce} = 2.5V$, $V_{bc} = 0.8V$. (a) $Wc = 0.1(\mu m)$, (b) $Wc = 0.05(\mu m)$.

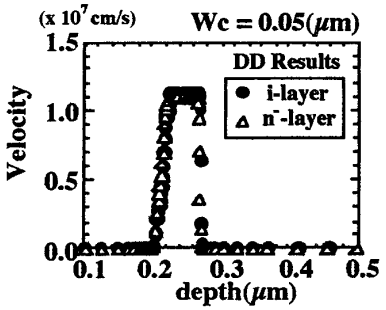

Fig. 4 Electron velocity in the $Wc = 0.05(\mu m)$ devic calculated by the DD simulation.

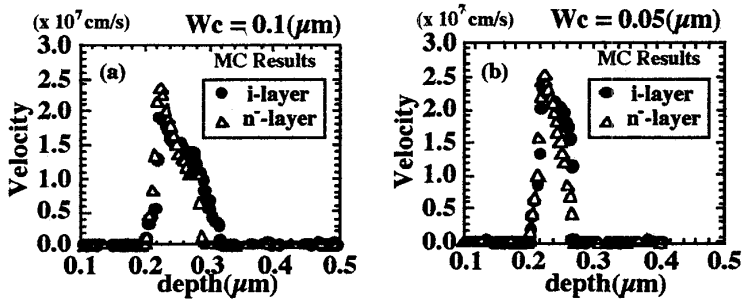

Fig. 5 Electon velocity obtained by the MC simlations. Strong velocity overshoots are observed near the BC junction for both n^-- and i-layer structures.

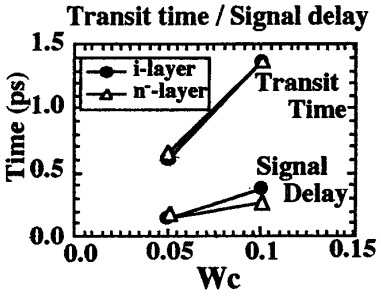

Fig. 6 Collector transit time and signal delay vs. Wc

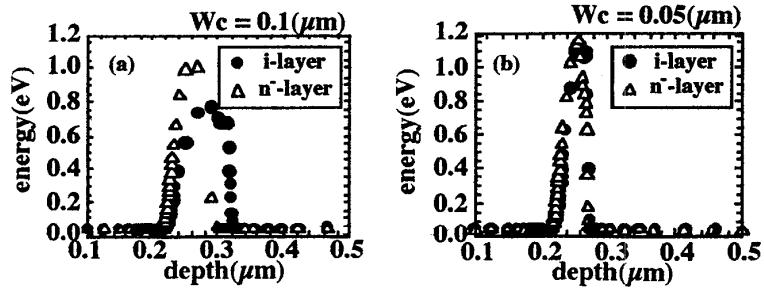

Fig. 7
Electron mean energy calculated by the MC simulation: The positon and the peak values are almost the same fo both the n - and the i-layer cases in $Wc = 0.05(\mu m)$ devi