A Simulation Strategy for Process Optimization

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Abstract
This paper presents an integrated process and device simulation framework aimed at optimizing the process parameters in view of a set of desired electrical performances. In addition the process design is driven in a direction as to minimize the sensitivity of the electrical performance characteristics towards process variations and/or fluctuations. The techniques used for achieving the objectives of the framework are based on Design of Experiments (DOE), Response Surface Methodology (RSM), and Target Oriented Design (TOD).

Introduction

Given the wide choice and complexity of ULSI process and circuit options, it is now widely recognized that an extensive amount of simulations is required to develop new processes [1]. However at the same time there is a need for a software framework that guides the process engineer, who is in most cases not that familiar with the details of software systems and simulations, in a robust, user-friendly and efficient way through the sequence of simulations to be performed. The decisions to be taken in process design are not only related to electrical device characteristics at the intrinsic device level but also to circuit performance, technology options and economics.
Today a wide variety of integrated software frameworks have been presented already. The VISTA framework [2], has the provision of a powerful interaction language and an efficient database system as its primary goals. Also the Process & Device Workbench (PDW) of NEC [3] and the PREDITOR system of CMU [4] do focus on issues related to creating the robust, easy to use environment. The US TCAD initiative [5] puts emphasis on standardizing the software related issues in integrating several pre- and postprocessing codes , simulators and user interfaces.
On a commercial level STUDIO of TMA [6] and the Virtual Fab of Silvaco [7] have been announced. These two frameworks also have easy, friendly to use and nice looking systems as a first goal.
The system that will be presented here is primarely aimed at enhancing the functionality of a framework for process optimization and provides therefore unique features which are not offered by the other systems. The first attempts for process optimization were undertaken in 1988 by A. Alvarez et al. [8].The system developed at IMEC contains several enhancements of the ideas initially described in that work. In section 1 the NORMAN/ DEBORA framework [9,10] will be presented. In section 2 an example of process optimization of a 0.5 um CMOS process will be given. Section 3 covers an example of the use of the framework in an industrial environment . Finally conclusions will be drawn in section 4.

1.The NORMAN/DEBORA framework

The problem the process engineer is faced with when designing a new process is schematically shown in figure1.The TCAD system we developed for solving this problem is presented on figure 2 and consists of 2 main parts: NORMAN and DEBORA. NORMAN focuses on the automatic sequencing and scheduling of a variety of simulation tools, using advanced DOE and very powerful RSM techniques. The user only has to specify the technology file, the device description, the variables or input factors (implant doses, energies, time, temperatures...), the range of the input factors,the target specifications and the experimental design chosen (Plackett-Burman, full/fractional factorial design, central composite faced, random/Latin-hypercube,target oriented...). NORMAN then takes care of all the process and device simulations to be conducted for all the experimental conditions . Process simulations are performed for all the relevant wafer cross sections constituting the devices under study (e.g in a CMOS process, the

NMOS and PMOS active and field transistors). Device simulators generate the measurements of the specified performances (threshold voltage, saturation currents, bulk factors...). The responses NORMAN handles however can also be figures of merit of comparison of simulated and user-specified X-Y data. With RSM the set of responses is then used to generate analytical functions for describing the relationship between the input variables and the responses. The analysis of the results may lead to an elimination of less significant input variables (screening). If appropriate NORMAN also looks for a transformation of the input variables which improves the model accuracy.
The DEBORA (DEsign Based Optimizer for Research Applications) part is a non-linear multi-response and multi-parameter optimization environment focusing on the final variable parameter optimization taking into account specified target and parameter ranges, thereby minimizing a weighted target error and/or target sensitivity objective function.For the time being the objective function is modelled as a Taylor series expansion, but other schemes are under study.
The combined use of NORMAN/DEBORA guides the process engineer towards optimal process variable settings, thereby meeting all specified requirements and minimizing the performance sensitivity towards process fluctuations and thus maximizing yield.
A special concept used in both NORMAN and DEBORA is Target Oriented Design (TOD). This technique is used to drastically reduce the number of computer runs to be performed. It consists of performing a directional search starting from a very restricted initial matrix. The directions in which the experiments seem to give the best fit to the target performance values are retained. The central points of these directions and if needed a number of less favourable directions are used as additional experiments to generate a second order analytical model, valid within the constraint region, which then can be used for screening.
Both NORMAN and DEBORA offer the possibility of calculating performance distribution functions by adding Gaussian "noise " profiles to each of the selected process and/or device input variables.
At this stage 2 important remarks have to be made. First, a powerful framework like NORMAN/DEBORA , which relies on simulators needs to be calibrated towards experimental results . Therefore modules are being added which evaluate the fit between experimental and simulated values and fine-tune the appropriate process or model parameters accordingly. Second, although the sytem is being presented here in a semiconductor processing environment, it should be emphasized that the software is being built in such a way as to facilitate the incorporation of any user specific simulator .

2. Example for a CMOS 0.5 um process optimization

The NORMAN/DEBORA framework has been used for the optimization of a 0.5 um CMOS proces. As input factors we retained 15 process variables (table 1) and we identified 6 responses (table2). Initially 17 points were choosen in the parameter space using a two level resolution III fractional factorial design. Then we started the TOD strategy, and added midpoints of " good " directions and "not too bad" directions to end up with a total of 136 points , just enough to build a second order interpolating model. That model was used for screening. After screening, 7 factors were judged to be relevant (table3) .Then a more complete CCF design was constructed, the results of which lead to refined models which were used as input to the optimization exercise of DEBORA. Equal weights were given to the target performance function and sensitivity function.
Histograms of Vt and the gamma factor for an initial point (= one of the midpoints of the TOD approach) and for the optimized point can be seen on figure 3 for the NMOS and on figure 4 for the PMOS device.The optimal design achieved a better centering of the Vt performance, a slightly narrower distribution (= decreased sensitivity) at the expense in some cases of a minor performance decrease (the gamma of the PMOS).
The latter illustrates the trade-offs to be made in real semiconductor processing.

3. An industrial example

That the presented framework is not only a research tool has been demonstrated by SGS-Thomson Microelectronics at Agrate [11]. They made full use of the analytical formulas

resulting from the RSM technique which at that stage are for the ranges considered an accurate replacement of the more CPU time consuming process and device simulators. The formulas are used to calculate the statistical distribution of the relevant responses with a realistic distribution of process variables as input (e.g. for the substrate concentration the in-coming specs were taken as extremes of a uniform distribution, for temperatures a +/- 10 degrees range was considered).A fine-tuning of the process parameters using experimental results was done. As an example of results obtained for a CMOS twin tub process, a comparison of simulated and measured Vt distribution of the n-channel at a VBS of - 5Volts is seen on figure 5. Figure 6 represents the importance of the different process factors for the p-channel Vt.

4. Conclusions

A very powerful tool for efficient and fast process optimization given all constraints imposed by real life has been presented. In addition to optimization it provides analytical relationships between input and output variables which can be used for statistical studies. On their turn these statistical distributions can serve as input variables in a similar exercise coupling also circuit simulators into the system. It is envisaged to explore that route in the near future. The OPEN SYSTEM software design principle used in developing the framework allows for application and user specific incorporation of other simulation programs not necessarely related to the microelectronics world.

Ackowledgments

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Factors	NAME	Nom	Low	High
1	n-well dose	1.6E13	0.5E13	2.5E13
2	n-well drive t1	60	30	90
3	n-well ox. t2	170	140	200
4	n-well drive t3	150	120	180
5	p-well dose 1	0.8E13	5.0E12	2.0E13
6	p-well drive t1	150	120	180
7	p-well dose 2	0.8E13	5.0E12	2.0E13
8	p-well drive t2	30	20	40
9	field ox. t	150	120	180
10	gate ox.t	15	15	20
11	n-LDD dose	6.0E13	5.0E13	1.0E14
12	p-LDD dose	6.0E13	5.0E13	1.0E14
13	LDD drive t	30	20	40
14	n-HDD dose	4.0E15	2.0E15	8.0E15
15	p-HDD dose	4.0E15	2.0E15	8.0E15

Table 1: Process variables and ranges

Constr	Name	Low	High	Target
1	nmos Vt	0.6	0.7	0.65
2	pmos Vt	-0.7	-0.6	-0.65
3	n-gamma	*	0.9	*
4	p-gamma	*	0.7	*
5	log nleak	*	-10	*
6	log pleak	*	-10	*

Table 2: Response constraints

Factors	Name	Nom	Low	High
1	nwell d	1.6E13	0.5E13	2.5E13
2	pwell d1	0.8E13	5.0E12	2.0E13
3	pwell t1	150	120	180
4	pwell d2	0.8E13	5.0E12	2.0E13
5	gate ox t	15	15	20
6	n-LDD d	6.0E13	5.0E13	1.0E14
7	p-LDD d	6.0E13	5.0E13	1.0E14

Table 3: Significant process variables/ranges

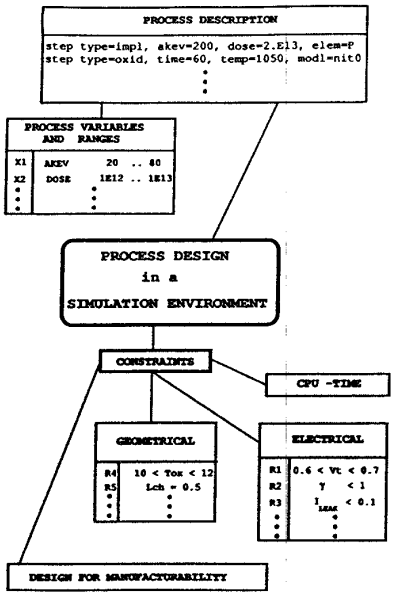

Figure 1: Problem description in process optimization

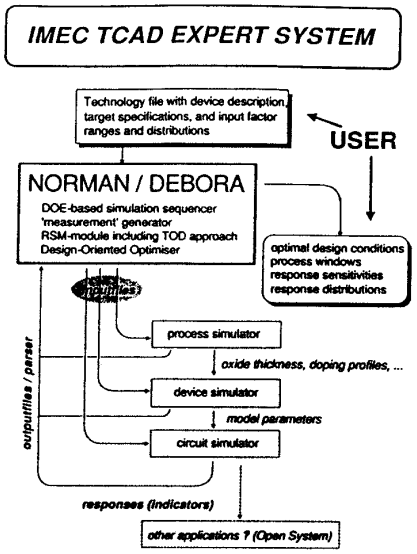

Figure 2: The IMEC TCAD NORMAN /DEBORA framework

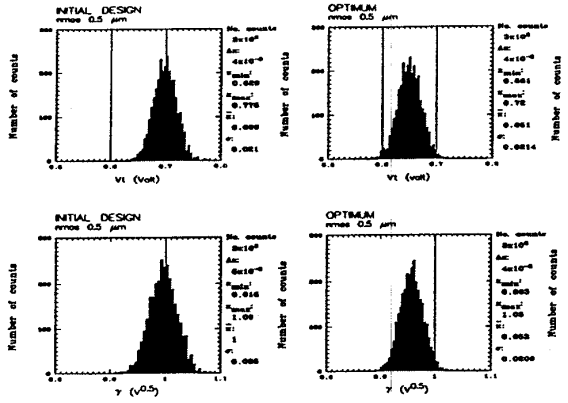

Figure 3: NMOS response distributions

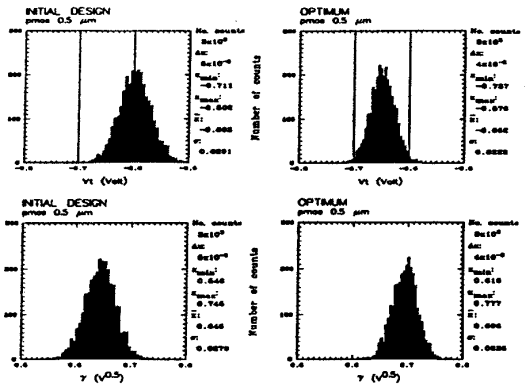

Figure 4: PMOS response distributions

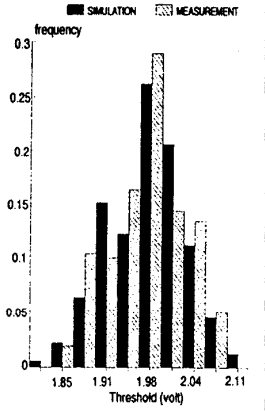

Figure 5: Measured and simulated NMOS Vt distribution

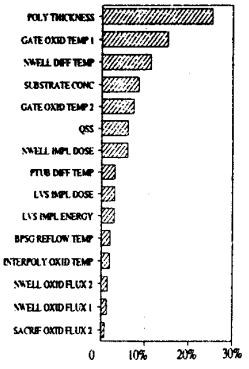

Figure 6: Relative weight of the input factors on PMOS Vt