Two-dimensional modeling of self-aligned silicide process with a general-purpose process simulater OPUS

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INTRODUCTION

In order to reduce source/drain resistance with shallower junction, self-aligned silicide(salicide) process was developed and is finding more applications to MOSFETs. Now, MOSFET process simulation including salicide process is a necessity. However, there have been few reports on salicide simulation mainly because the implement of 2D model is very difficult.

We have developed a 2D salicide process model in a general-purpose process simulator OPUS[1]. An analytical model which takes the device topography into account is developed for reaction of metal and Si. The thorough 2D simulation of MOSFET process could be one of the first to be reported ever.

MODELS

The growth model of silicide is schematically shown in fig.1. Silicide growth due to metal-Si reaction is based on the following equation[2]:

$$L^2 = At \exp(-E_a/kT), \qquad (1)$$

where t is the time, E_a is the activation energy, kT is the energy, and A is a constant. L is an effective thickness of a silicide layer, considering 2D topography as shown in fig.1. When growth takes place at metal/silicide (M/MS) interface, the growth rate at point P is calculated by using a minimum length (L_G) from P to silicide/Si (MS/S) interface. Concomitantly, silicon consumption takes place at MS/S interface. The consumption rate of Si at point Q is also calculated by eq.(1) using a minimum length (L_C) from Q to M/MS interface. Finally, the increment of volume reduction in Si is balanced considering total number of consumed silicon and metal. Although the above explanation is for the silicide growth due to silicon out-diffusion, the model can account for metal-diffusion limited growth of silicide. Impurity diffusion model includes the analytical enhanced diffusivity model based on point-defect generation, and segregation at the interface.

These models are implemented in OPUS, and 2D process simulations of the thorough MOSFET including salicide process are successfully carried out.

SIMULATION RESULTS

We show here an example of 2D PMOSFET simulation with Ti-salicide process. Fig.2(a) and (b) show the device structure before and after silicidation anneal at 650° for 60 sec., respectively. The thickness of Ti is 50nm. We can see a TiSi2 spike on the spacer. This is explained by silicon-diffusion limited growth of a TiSi2 layer[2], and is well simulated by OPUS.

Fig.3 shows a depth profile of B before and after salicide anneal, and after final anneal at 900° for 15min. Also shown is B profile without salicide process. Just after salicide anneal, almost all of B is segregated into TiSi2 layer[3]. During final anneal, interfacial flux from Si to TiSi2 is significant, increasing B concentration in TiSi2 near MS/S interface. Near TiSi2 surface, B outdiffuses toward SiO2, decreasing the surface concentration. Since no enhanced diffusion is assumed in Si with TiSi2, junction depth with TiSi2 is smaller than that without TiSi2 due to TiSi2-bound flux.

CONCLUSION

We have developed a 2D salicide process model in OPUS, and succeded in thorough simulation of PMOSFETs with Ti-salicide process. The simulations well explain the reported results, proving the efficiency of the new model.

REFERENCES

[1] K.Nishi et al, IEEE Trans. CAD-8, 23, (1989)
[2] P.Revesz et al, J.Appl.Phys. 54, 2114 (1983)
[3] D.L.Kwong et al, J.Appl.Phys. 61, 5084 (1987)

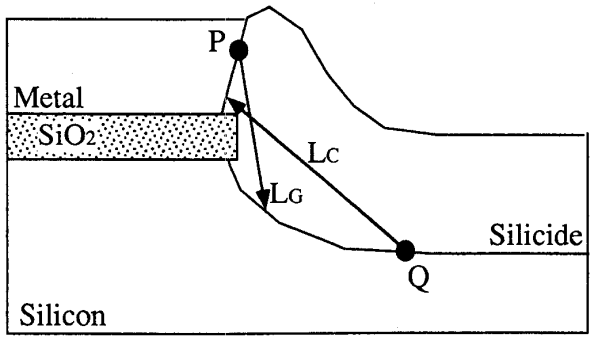

Fig.1: Effective silicide thickness for 2D silicide growth calculation

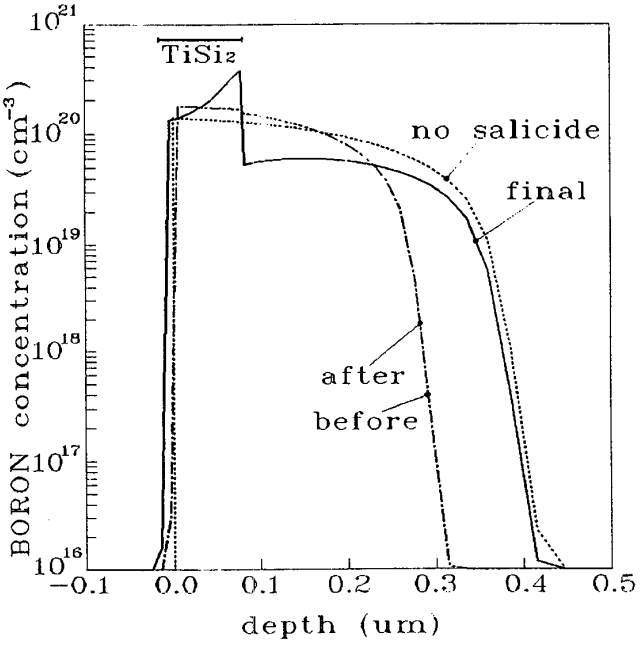

Fig.3: Depth profile of B at source /drain

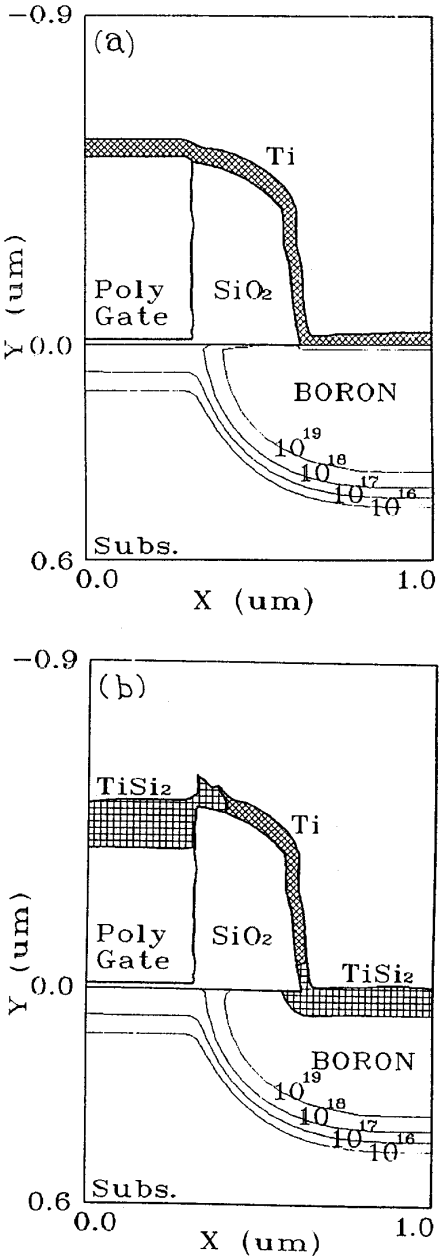

Fig.2: Simulated PMOSFET structure; (a) before silicide anneal, and (b) after silicide anneal