A System for 3 D Simulations of Complex Si and Heterostructure Devices

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INTRODUCTION: The simulation of three-dimensional effects in semiconductor devices has gained in importance as characteristic device dimensions shrank to submicron size. Moreover, complex device geometries, e. g. trench-stacked capacitors used for DRAM's, are inherently three dimensional, and can thus not be simulated in 2 D. In the past decade, the solution of the semiconductor equations in 3 D within the drift-diffusion model has been investigated by many authors. We have developed a 3 D device simulator which features several improvements compared to previously published approaches: (1) The device geometry is defined using an interactive geometric modeler developed on purpose. As a result, many kinds of complex 3 D geometries can be defined and modified easily and quickly. (2) The grid allocator generates tetrahedral grids, thus leading to an optimal allocation of grid points. Moreover, topologic transformations are applied to obtain a grid suitable for the control volume integration method; thus, the well-known "obtuse angle problem" is avoided without injecting a large number of redundant grid points. (3) The simulator solves the device equations both for silicon and heterostructure devices. (4) The geometric modeler and grid generator can also be used as preprocessors for wire capacitance and resistance calculations. In the following, we shall outline the different components of our simulation system, shown in Fig. 1.

INPUT OF DEVICE GEOMETRY: The device geometry is defined with an interactive geometric modeler. The user draws simple polygons, which are then swept to obtain rectangular prisms. Next, the prisms are automatically assembled through boolean operations: if two prisms belong to the same material region, their boolean union is computed; otherwise, we take their boolean difference (Fig. 1). The result is a description of the boundary and of the internal material interfaces of the device to be modeled. We consider this approach a reasonable trade-off between ease of use and flexibility, since many kinds of 3 D geometries can be modeled (or reasonably approximated) by assembling rectangular prisms; on the other hand, a modeler capable of handling any 3 D plane-faced geometry would be much harder to use (and to implement).

GRID ALLOCATION: The grid generation process is subdivided in two steps [1]. First, an initial tetrahedral grid is generated, using a modified finite octree approach. This grid fits the device boundary exactly, and point density is adapted to the impurity gradient and according to some user-provided parameters. Then, "3 D obtuse angles" are eliminated through "3 D edge swapping": if for some grid point appropriate non-overlapping control volumes can not be defined, the grid topology is locally modified (Fig. 1). New points are injected only when no appropriate topologic transformation is available, thus minimizing the number of redundant grid points.

SOLUTION OF DEVICE EQUATIONS: The Poisson and current continuity equations are solved using a classical control volume integration scheme. The equations can be solved either one after the other (decoupled scheme), or simultaneously, using a full Newton scheme. The linearized equations are solved with Bi-CGSTAB, a preconditioned conjugate-gradient-like iterative scheme. Both steady-state and transient simulations can be performed with our simulator. Heterostructure simulations are performed with band parameters for each material [2]. Wire capacitance calculations are based on the charge value, computed with Gauss' theorem [3]. Wire resistance calculations are done analogously.

RESULTS: The examples in Fig. 2 illustrate the capabilities of our simulator. Thanks to the interactive preprocessor, each of these structures could be easily defined. Figure 2 (left) shows the geometry and grid for a MOSFET. Figure 3 (left) compares the I-V characteristics of the 3 D MOSFET and of a 2 D cut through the same structure. The offset of the two curves is due to the narrow channel effect, visible only in a 3 D simulation. The middle structure in Fig. 2 shows the grid for a heterostructure bipolar transistor. Again, Fig. 3 (right) compares the currents for the full 3 D structure with those of a 2 D slice of the same HBT. While the emitter currents are virtually identical for both structures, a 3 D effect is noticeable in the base currents. Finally, Fig. 2 (right) shows a structure for which we have performed some wire capacitance calculations. These examples indicate that the present system is both a practical and valuable tool for the investigation of state-of-the-art semiconductor devices.

REFERENCES:

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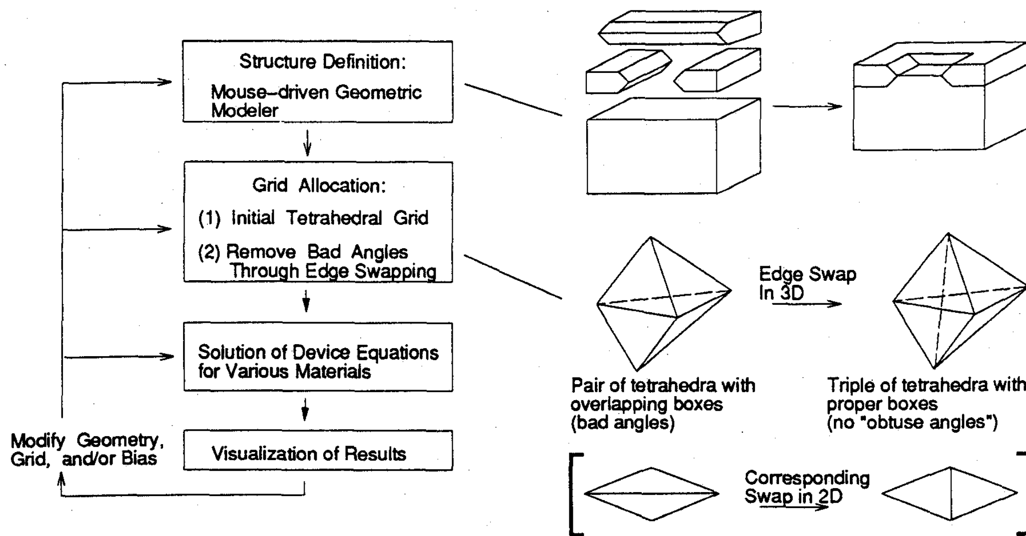

Figure 1: Overview of 3 D simulation system.

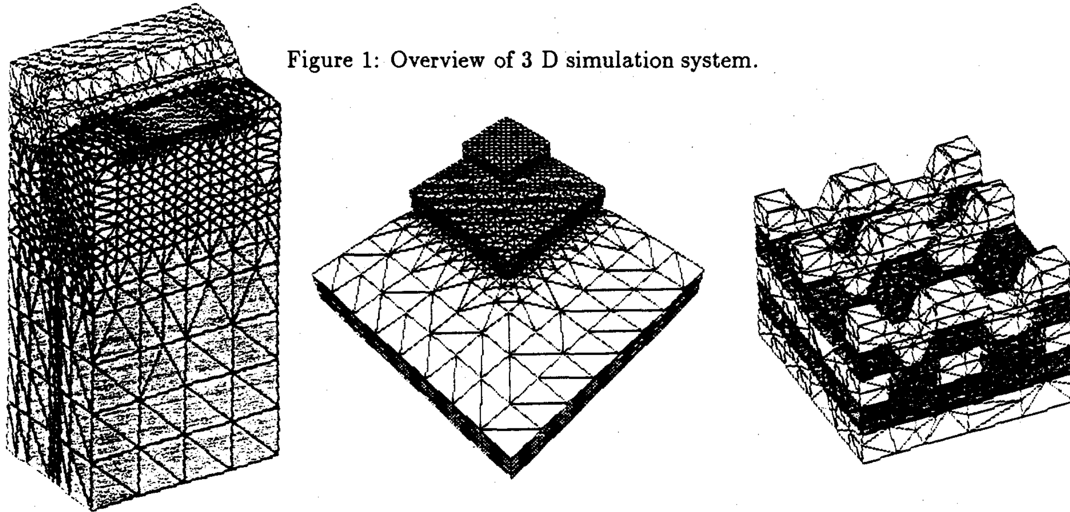

Figure 2: Grids for MOSFET (left, 6310 grid points), HBT (middle, 7080 points), and for structure for wire capacitance calculations (right, 1340 points, metal wires white).

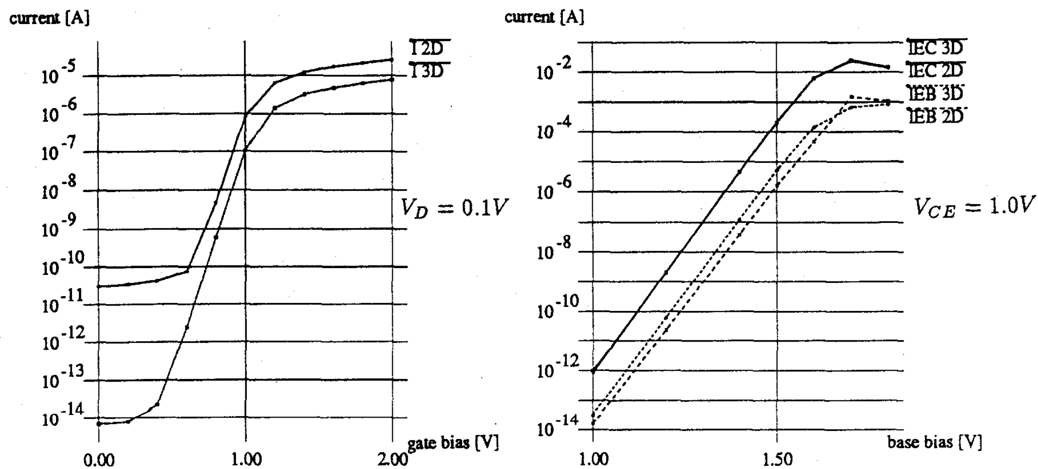

Figure 3: Contact currents *vs.* bias voltage for MOSFET (left, lower curve 3 D MOSFET, upper 2 D slice) and HBT (right, IEC 3D = $I_{collector}$, IEB 3D = I_{base} for 3 D HBT, IEC 2D & IEB 2D for 2 D slice).