Failure Mechanism of PN Junction caused by EOS

Y.Tajima, K.Asada, and T.Sugano
The Faculty of Engineering, The University of Tokyo

1 Introduction

Effective ways have been desired to protect the integrated circuits(IC) from the electrical over stress(EOS), as the scaled IC becomes more susceptible to damages due to EOS; the pn junction burnout. Mechanisms of the junction burnout have been studied by many researchers[1 9] mainly in terms of the relation between pn junction structures and the minimum EOS power for the destruction of the junction[6 9]. The study of Wunsch&Bell[10] is especially well known among these results. It should be noted, however, that these studies were done using one dimensional and uniform breakdown models. There are still several unclear phenomena for the breakdown of two dimensional device structures, such like the *planar* type junctions[11, 12].

In this paper, we describe numerical simulation results of the relations between the minimum EOS power to failure and the time to failure, for various two dimensional *planar* junction structures.

2 Numerical Analysis of Failure Mechanism

A. Simulation Methods

We adopted a pseudo two dimensional model where a pn junction diode is divided into small elements and represented by a circuit network composed of many minute resisters and diodes as shown in Fig.1. Simulation procedure used is described in Fig.2. It is an iterative method so that the estimation of the values of the resisters is carried out utilizing a temperature distribution obtained at the previous step, and then voltage distribution is calculated until converged. The initial temperature is a room temperature. The power dissipation in the minute resisters and diodes is used as the heat source of the two dimensional transient heat conduction equation, which is again represented by a network similar to Fig.1.

We are assuming that the device is destroyed when the junction temperature reachs some predefined temperature; the intrinsic temperature. The empirical formulas[13] are used for the dependence of the carrier mobility on the electric field or temperature, and the dependence of the heat conductivity or breakdown voltage on temperature.

B. Simulation Results

Typical simulation results are shown in Fig.3. When the impurity concentration in the substrate is high enough (e.g. $N^{-}_{sub} = 10^{17}$[cm ^{3}]), the relation between the failure power and the failure time coincides with the Wunsch&Bell model; the failure power proportional to about (the failure time)$^{-\frac{1}{2}}$ in the region of $10^{-7} \sim 10^{-6}$ sec. On the other hand, when the impurity concentration in the substrate is low enough (e.g N^{-}_{sub} 10^{16}[cm^{-3}]), the failure power is in proportion to about (the failure time)$^{-\frac{1}{3}}$. It can be understood that the temperature distribution of the pn junction is governed by a different mechanism depending on the impurity concentration.

We examined the dependence between the width of current path in the depletion layer and the gradient of the curve of the failure power versus failure time, using a device structure shown in Fig.4a. A strong correlation was observed between the path width and the average gradient in the region of $10^{-7} \sim 10^{-6}$ sec., as shown in Fig4.b. When the current path is wider than 10.0μm, the power is in proportion to (the failure time)$^{-\frac{1}{2}}$, while the power is in proportion to (the failure time)$^{(-\frac{1}{4} \sim -\frac{1}{3})}$, when the current path is narrower than 1.0μm.

3 Discussion

The breakdown spot in a diode depends on the device structure. Shift of the breakdown spot is considered as the main reason of the differences in the relation between the failure power and the failure time, described above. When the impurity concentration in the substrate is high enough, there is little difference between the breakdown voltages at the junction edge and the junction body. So the breakdown occurs simultaneously at the whole junction. The heat diffusion is governed by an uniform heat source at the whole junction, as if a dimensional mode. When the impurity concentration in the substrate is low enough, the breakdown occurs only at the junction edge because of the relatively higher resistance in the substrate. The heat generation in the depletion layer is not uniform in this case, because of the current concentration at the edge. The heat transfer should be treated as two dimensional.

In a realistic situation, if the breakdown voltage of a local part of the junction is much lower than that of the other, for instance, because of a junction defect, the breakdown occurs only at this weak point, no matter how the impurity concentration in the substrate is. It can be anticipated that the failure power is in proportion to about (the failure time)$^{-\frac{1}{3}}$ because of the two dimensional heat conduction.

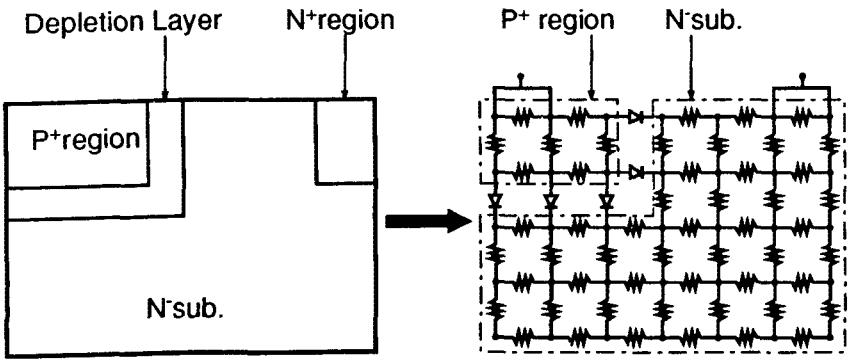


Fig.1 Model figure of diode-resister network.

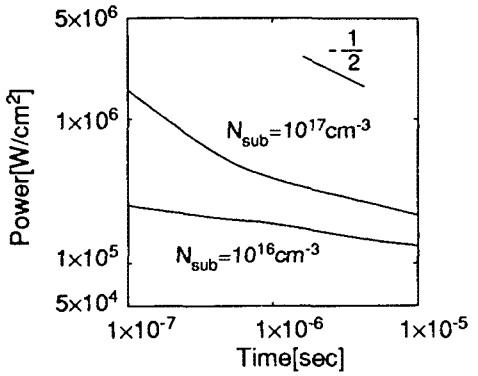


Fig.3 Calculated failure curve for *planar* junction.

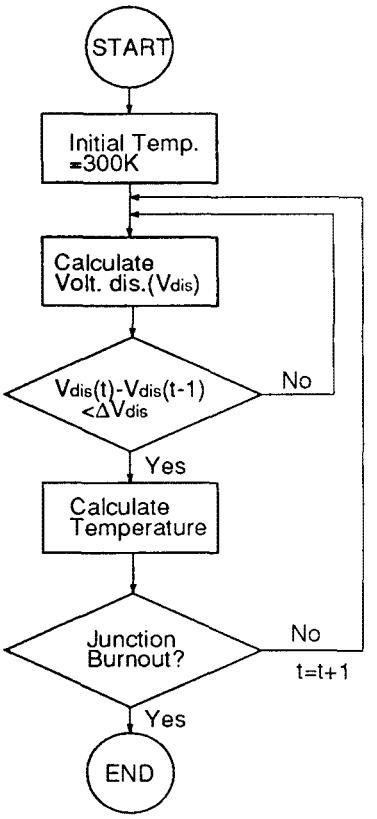
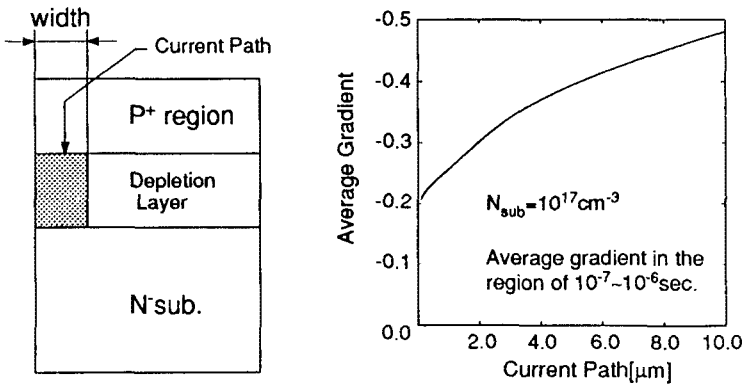


Fig.2 Flow chart of calculation



(a) Model structure (b) Calculation results

Fig.4 Average gradient of the failure curve in $10^{-7} \sim 10^{-6}$sec.

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