Simple Model of MOSFET Breakdown Characteristics: from Saturation to Snapback Sustaining Regime.

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The interest in snapback modeling usually comes from designers of EPROMs where it constitutes an acute constraint. Recently snapback has also found some useful applications such as input/output ESD (electrostatic discharge) protection circuits, thus further rising a need for a reliable snapback model. In the literature there are merely a few phenomenological studies on snapback, e.g. [1], and even fewer models, here [2] seems to be the only example. The problem with this model, however, is its inaccuracy and the lack of a snapback criterium. Both [1] and [2] prove that snapback must inevitably occur but do not point out what is the precise impulse which leads to its triggering at the very particular and reproducible point of the characteristic. The present paper is an extension (to snapback region) and simplification of our previous physical studies [3] and [4] on the multiplication -induced breakdown.

Enhanced body effect. According to [3] and [4], the first phase of the breakdown consists in a lowering of the threshold voltage caused by a positive biasing of the bulk spreading resistance by the substrate current I_{sub}. This lowering is similar in its nature to the body effect but considerably enhanced due to the presence of a non-vanishing electrical field in the bulk, which does not occur in the ordinary body effect. In the present paper we propose a new CAD model for the threshold voltage including the enhanced body effect along with all the other effects (short and narrow channel, non-uniform doping, drain and bulk biases), which V_{th} is subject to, in the form of a single closed form expression. As shown in Fig. 1, the enhanced body effect allows a better fit to the measured data than the ordinary body effect, and may lead alone (with the parasitic bipolar transistor still being turned-off) to a considerable up-bending of the characteristic.

Parasitic bipolar action. The expansion of the EPR (equipotential region being also the base of the parasitic bipolar transistor (BT)), has been shown in [3] to be the key point in the bipolar action. In this paper we propose to account for this expansion by means of two parasitic BTs: a high gain and constant geometry BT (corresponding to the upper part of the EPR) and a very low gain and variable geometry BT (the lower part of the EPR). The latter is considered to degenerate into a diode ($\alpha \rightarrow 0$) for the sake of simplicity. The corresponding equivalent circuit and resulting drain current expression are shown in Fig. 2. Fig. 3 illustrates that it is impossible to neglect the expansion of the EPR and thus to account for the breakdown physics in terms of a single, constant gain BT, as has previously been attempted e.g. in [5].

Snapback. As snapback can only occur in current-drive conditions, we have thus extracted the multiplication coefficient M as a function of I_D (see Fig. 4) from the current balance (Fig. 2). The obtained expression is very suitable for the analysis of snapback since there is a direct correspondence between M and V_D. Fig. 4 shows that indeed, as M is a monotonically increasing function of V_D, any variation in M (with I_D) imprints its image on V_D. Before snapback, P (defined in Fig. 2) increases faster than I_D, mainly because of the increase in I_{sub} (channel current I_{ch} levels-off before). As a result, M, and thus also V_D, both rise with I_D, compare Fig. 4. At a certain point, however, I_{sub} has been found to saturate (or at least to change considerably slope, see Fig. 5), which causes P/I_D to peak and then to turn down, thereby leading to a reduction in M. Consequently V_D also starts to decrease (triggering of snapback) with a further increase in I_D, see Fig. 4. This brings the MOSFET into a strong positive feedback regime. The decrease in M further increases I_D (see I_D expression in Fig. 2, with $P \cong \text{const}$ and $d \approx \text{const}$ (close to 1) as is the case in snapback) which in turn reduces M even more, etc,etc..., this being the essence of snapback. In this way I_D tends very quickly to infinity, thus bringing M to its limiting value $M_{sus}=(1-\alpha)/\alpha/(1-d)$. M_{sus} can be easily transposed into the corresponding V_{sus} value, by means of the $M \approx \mathcal{M}(V_D)$ relationship provided by any reliable multiplication coefficient model (in this work a model based on [6] and developed in [7] has been used). V_{sus} voltages predicted in this way, as well as entire breakdown characteristics, agree very closely with measured data, as shown in Fig. 6. It is interesting to see that the saturation of I_{sub}, being the crux of the snapback physics, is also a result of the EPR expansion.

Substrate current. As shown in [3], the initially downward expansion of the EPR becomes more and more lateral, as it encroaches below the source and drain domains, thus resulting in a saturation of R_{sub} and consequently also I_{sub}. A simple and explicit substrate current model derived from the above considerations can be seen in Fig. 6, to be in very good agreement with the measured data. Due to the non-zero source series resistance r_s, the saturation of I_{sub} may be imperfect in spite of a distinct saturation of R_{sub} (see Fig. 5). Nevertheless, the triggering of snapback is still determined by the saturation of R_{sub}, thus providing a simple snapback criterium $R_{sub} \rightarrow R_{trig}$. In addition, R_{trig} has been found to be constant in a wide range of channel lengths and gate biases, thus confirming its usefulness as a snapback criterium.

In conclusion we would like to emphasize that the saturation of R_{sub}, proved theoretically as well as experimentally, provides a very simple and general snapback criterium (which has been lacking to date). The new concept of a parasitic BT plus a diode together with the new threshold voltage model (including the enhanced body effect) have turned out to be successful, ensuring a good accuracy (error of the order of 3%) and a high degree of simplicity. The proposed new V_{th} model is expected to be the most compact and general among those available at present.

References

[1] B.A. Beitman, IEEE Trans. Electron Devices, vol. ED-35, pp. 1935-1941, Nov. 1988.
[2] Fu-Chieh Hsu *et al.*, IEEE Trans. Electron Devices, vol. ED-29, pp. 1735-1740, Nov. 1982.
[3] T. Skotnicki, G. Merckel and A. Merrachi, in IEDM Tech. Dig., pp. 87-90, 1989.
[4] T. Skotnicki, G. Merckel and A. Merrachi, to be published in Solid State Electronics.
[5] Fu-Chieh Hsu *et. al.*, IEEE Trans. Electron Devices, vol. ED-30, pp. 571-576, June 1983.
[6] H. Martinot and P. Rossel, Electronics Letters, pp. 118-120, March 1971.
[7] A. Merrachi, Ph.D. thesis, CNET-CNS, France, September 1990.

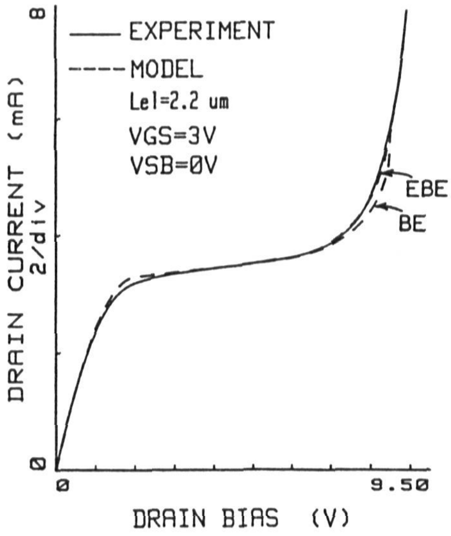
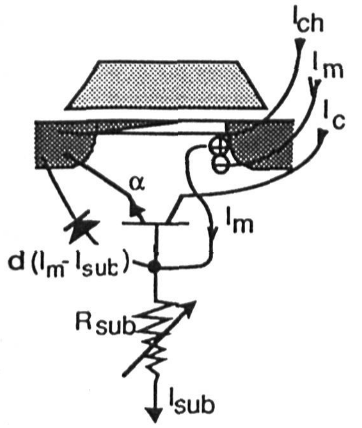


Fig. 1. Modeled (broaken lines) and measured (solid line) I_D versus V_D characteristic. A replacement of the body effect (BE) by the enhanced body effect (EBE) improves accuracy.



$$I_D = \frac{(1+M)P}{\alpha[1+(1-d)M]-1}$$

$$P = \alpha(1-d)I_{sub} - (1-\alpha)I_{ch}$$

$$d = \mathfrak{D}\downarrow(R_{sub}) \in (0,1)$$

decreasing function

Fig. 2. Equivalent circuit and corresponding current balance equation. d accounts for the expansion of the EPR (base).

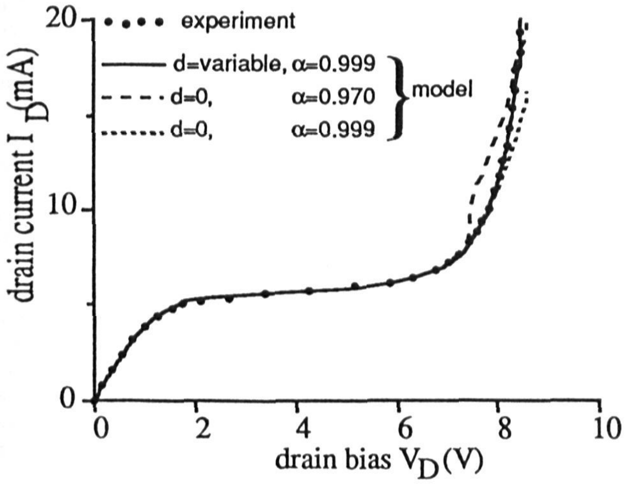


Fig.3. Modeled and measured drain output characteristics. At d=0 (single parasitic transistor scheme) no choice of α enables matching of the model with the measured curve.

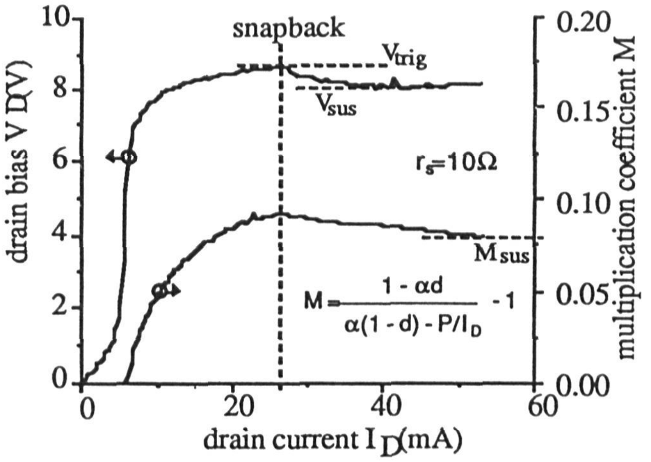


Fig. 4. Illustration of the direct correspondence between the drain bias V_D and the multiplication coefficient M. The curves have been extracted from measured data taken on a MOSFET of L_{el}=1.2μm and Z=50μm at V_G=3V.

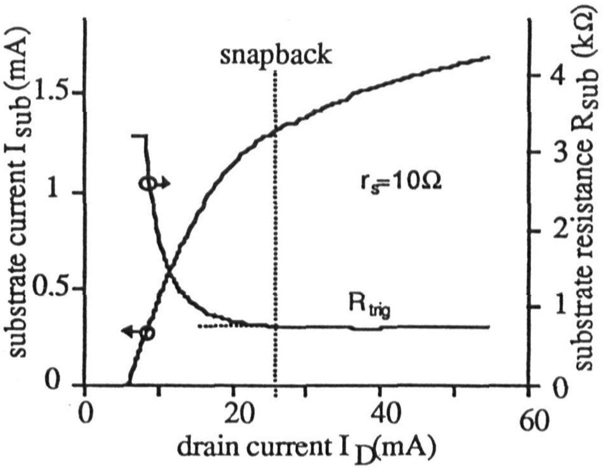
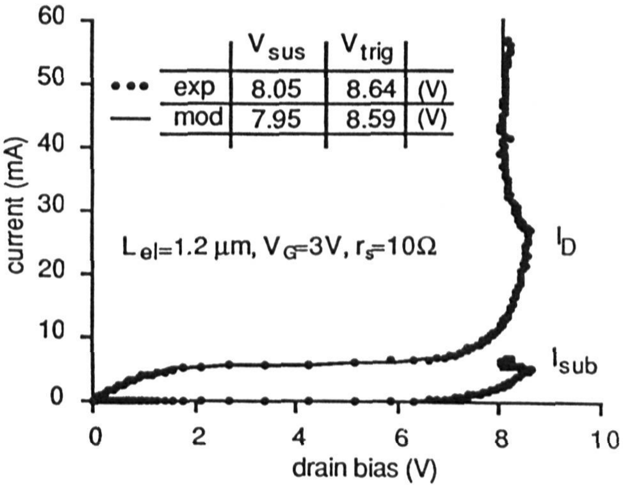


Fig. 5. Measured substrate current and substrate spreading resistance versus drain current. The bottoming-out of R_{sub} determines very well the triggering of snapback. The dotted vertical line indicates the snapback triggering, as read-out from measurements. L_{el}=1.2μm, Z=50μm and V_G=3V.



		V_{sus}	V_{trig}	
•••	exp	8.05	8.64	(V)
—	mod	7.95	8.59	(V)

Fig. 6. Comparison between measured and modeled snapback characteristics (drain and substrate currents).