CAPCAL V1.3: Electrical field calculation with appropriate pre- and postprocessing for VLSI applications

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Introduction: The following pre- and postprocessing capabilities render an electrical field calculator especially well suited for VLSI applications:
Extraction of conductance/capacitance network from potential distribution
Circuit analysis on this network
Extraction of 3D geometry from layout
Results of both, analysis of contact holes and substrate coupling of bipolar circuits are presented to demonstrate these features.

Analysis of contact holes

In [1] it was shown by 2D simulation that a correction of the extracted value of the contact hole resistance (R_{ce}=U/I) is necessary to obtain the resistance of the metal semiconductor interfacial layer. The post-processing capabilities of CAPCAL V1.3 allow for easy investigation of this effect in 3D.
From the Kelvin-structure (Fig.1) CAPCAL extracts an equivalent circuit of the form shown by Fig.2a. This circuit is transformed into an equivalent Y-circuit (Fig.2b) where the contact resistance appears as a series resistance at the contact #1.
The series-resistance Rs1 limits the accuracy of the interfacial resistivity measurement. CAPCAL can now be used to either optimize the design of the test-structure or to calculate an appropriate correction of the measured contact resistance value. Both ways will be discussed in the proposed paper. Examples will be given.

Substrate coupling in bipolar circuits

The parasitic coupling acts increasingly as a limiting factor in the design of high speed bipolar circuits. The most widespread method to limit this effect is the use of a shielding network. The technological realization of this network was analized and optimized by using CAPCAL V1.3.
A simplified ohmic model of the circuit was developed. The design-system was coupled to the preprocessor of CAPCAL to automatically extract the geometry-data from the layout. A test-structure was used to verify this model by conductance measurements between alu-pads. The simulation results were found to be within a 15% range of the measured values.

The model was used to optimize the design of the shielding network. The effect of an additional polysilicon line below the aluminum layer was investigated. The distribution of the electrical field is shown in Fig. 3 (a: no poly, b: with additional poly). The parasitic coupling between the transistors shown by hatched areas was found to vary by a factor of 2-3 depending on this technology variation.

REFERENCES

[1] W.M.Loh, K.Saraswat, R.W.Dutton, IEEE Electron Dev.Lett. Vol.EDL-6, No.3, Mar.1985

[2] A.Seidl, H.Klose, M.Svoboda, J.Oberndorfer, W.Rösner IEEE Trans. CAD Vol.7, No.5, May 1988

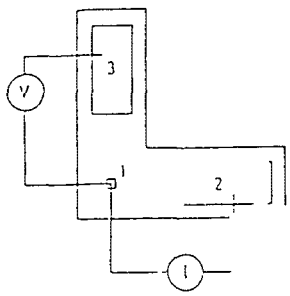
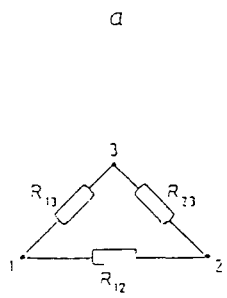


Fig. 1



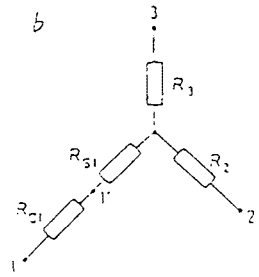


Fig. 2

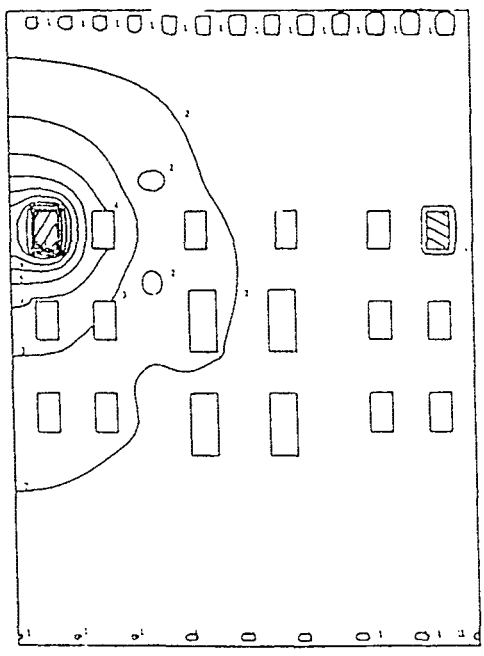


Fig. 3a

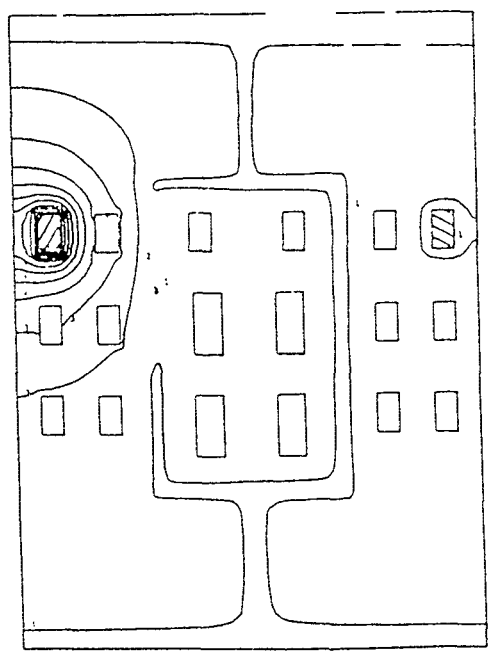


Fig. 3b