Three-Dimensional Evaluation of Substrate Current in Recessed-Oxide MOSFETs[1]

A. Pierantoni, P. Ciampolini, A. Gnudi and G. Baccarani
DEIS, Università di Bologna, viale Risorgimento 2, 40136 Bologna, Italy

In the last few years, several efforts have been made to overcome the main limitations of the "classical" two-dimensional, drift-diffusion model; on the one hand, more sophisticated transport theories have been worked out: among them, the hydrodynamic model [1] was given much attention, and two-dimensional simulators implementing such a model were developed. On the other hand, three-dimensional drift-diffusion codes have been written, with the aim of predicting new geometry effects related to the three-dimensional nature of real devices. However, energy-activated phenomena and geometry effects are likely to interact; hence the need for a three-dimensional formulation of advanced transport models [2]. In this paper, a "hydrodynamic" version of the three-dimensional code HFIELDS-3D is used to achieve a detailed knowledge on the distribution of the substrate current inside a recessed-oxide MOSFET.

In the current version, HFIELDS-3D solves the equations of the hydrodynamic model described, e.g., in [3]; the discretization technique proposed in [4] has been generalized to the three-dimensional case, using prisms as fundamental elements [5]. A single-carrier, coupled solution has been worked out for Poisson's and current-continuity equations, while an outer, decoupled loop takes care of the energy-balance equation. Temperature-dependent impact-ionization rates have been used, according to the model proposed in [6].

An MOS transistor with fully recessed isolation oxide was simulated using HFIELDS-3D. Fig. 1 shows its geometrical features as well as the discretization mesh. As shown by Akers [7], the edge effect in such devices lets the current crowd at the periphery of the channel, so that threshold voltage shifts downward. This is referred to as the "inverse narrow-width effect" (INWE). As impact ionization rate at the drain-end of the channel depends on current density, the substrate current is expected to be nonuniform across the channel as well. This straightforward consideration, however, does not fully justify the discrepancies between two- and three-dimensional simulation results shown in fig. 2, where much larger differences are found to occur in substrate current compared with drain current. The source of such discrepancies is made clearer in fig. 3, where the ratio:

$$Q = \frac{(I_B/I_D)_{3D}}{(I_B/I_D)_{2D}}$$

is plotted against gate voltage. By normalizing the substrate current I_B to the drain current I_D, one should in fact get rid of the effect related to the crowding of the drain-current at the device periphery: this plot, therefore, clearly demonstrates further three-dimensional features. Fig. 4 shows the electron temperature at the gate-oxide interface, which exhibits a sharp peak at the drain junction. At the channel edge, such a peak significantly increases: thus the lateral electric field is expected to be enhanced at that point. At low gate bias, the substrate current comes predominantely from this region despite its small spatial extension: fig. 5 shows the fraction of the substrate current which originates from the outer 15% of the channel and clearly supports the above statement. Finally, fig. 6 maps the ionization rate over the device geometry and shows the "hot spot" located at the corner. At higher gate voltages, the contribution of the edge region decreases, eventually reversing the above effect, as can be inferred from fig. 3. This can be clarified as follows: the recessed-oxide MOSFET can be viewed as being due to the parallel of two MOSFETs with different threshold voltages. At low gate voltage, where the substrate current increases against voltage, impact ionization occurs predominantely at the edge of the channel, where most mobile carriers reside. At large gate voltages, instead, the substrate current decreases in long-channel devices, due to the peak-field reduction which occurs as the device enters the triode region; therefore, one should expect the above discrepancies to reverse. In short channel MOSFETs, however, such a decrease, if any, is far less pronounced, and the lateral shift of the curve related to the edge effect may or may not be responsible for an intersection of the 2-D and 3-D curves, as shown in figure 2.

In summary, we have shown that the INWE is responsible for a pronounced three-dimensional enhancement of the substrate current in recessed-oxide MOSFETs. Self-consistent simulations were performed by solving the device equations within the so-called hydrodynamic model, i.e. by incorporating within the transport model an energy-balance equation. Results show that the narrow-channel effect has a different impact on drain and substrate currents; moreover, the non-uniform temperature distribution at the gate-oxide interface is likely to affect to some extent the gate current as well.

References

[1] K. Bløtekjær, *IEEE Trans. on Electron Dev.*, vol. ED-17, pp. 38-47, 1970.
[2] K. Katayama, T. Toyabe, *IEDM Technical Digest*, pp. 135-138, 1989
[3] M. Rudan, F. Odeh, *COMPEL*, vol. 5, pp. 149-183, 1986
[4] A. Gnudi, F. Odeh, *SISDEP Conference Proceedings*, pp. 387-390, 1988
[5] P. Ciampolini, A. Pierantoni, G. Baccarani, *IEEE Trans. on CAD of ICAS*, (to be published)
[6] E. Schöll, W. Quade, *J. Phys. C: Solid State Phys.*, vol. 20, pp. L861-L867, 1987
[7] L.A. Akers, M. Sugino, J. Ford, *IEEE Trans. on Electron Dev.*, vol. ED-34, pp. 2476-2481, 1987.

---

[1] This work was supported by CNR, under the "Progetto Finalizzato MADESS" and by ST Microelectronics S.p.A.

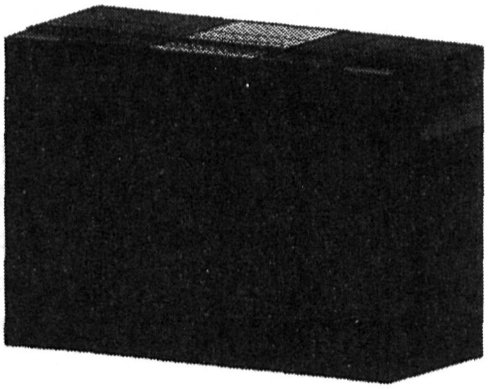

Fig. 1: The simulated device: the mesh counts 15.100 nodes. $L = 0.6\mu m$, $W = 0.8\mu m$.

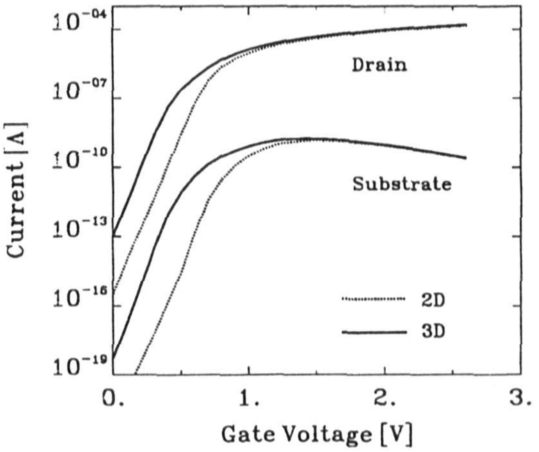

Fig. 2: I-V characteristics: $V_{DS} = 3V$.

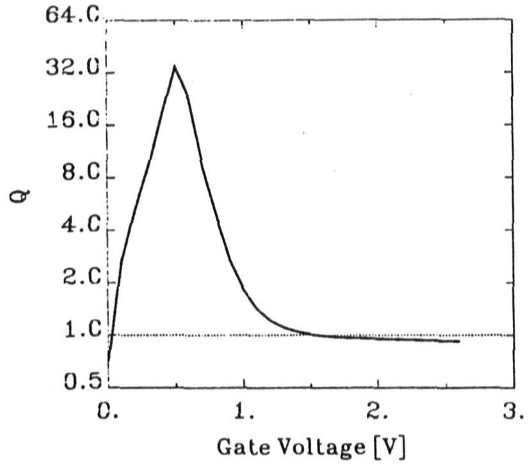

Fig. 3: Ratio between 3D and 2D normalized substrate currents: $V_{DS} = 3V$

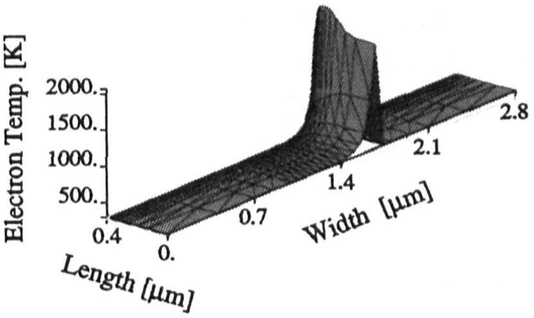

Fig. 4: Electron temperature distribution at the gate-oxide interface: $V_{GS} = 0.5V$, $V_{DS} = 3V$.

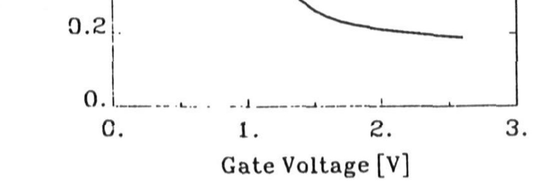

Fig. 5: Fraction of the total substrate current originating from the outermost region: $V_{DS} = 3V$.

Fig. 6: Impact ionization rates ([cm^{-3}·s^{-1}], log scale): close-up of the drain region (oxide has been removed). $V_{GS} = 0.5V$, $V_{DS} = 3V$.