Device-Level Analysis of a $1\mu m$ BiCMOS Inverter Circuit Operating at 77K

J. B. Kuo and Y. W. Chen
Dept. of Electrical Eng., National Taiwan University
Rm. 526, Roosevelt Rd., Sec. 4, #1, Taipei, Taiwan 107
Fax:886-2-363-8247, Telephone:886-2-363-5251, E-mail:kuojb@leibniz.ee.ntu.edu.tw

Abstract

This paper presents a device-level study on the steady state and transient behavior of a $1\mu m$ BiCMOS inverter circuit operating at $77K$ using a modified PISCES program, where appropriate low temperature device models with a large-scale simulation capability have been added. According to simulation results, at $77K$, the fall time is 35.2% longer and the rise time is about identical, compared to $300K$, due to a smaller output swing and a smaller non-negligible collector current in the BiNMOS transistor and a smaller BiPMOS emitter current at $77K$ during pull-up transient. Circuit and device designs can be optimized to justify the low temperature operation of BiCMOS circuits.

Summary

Recently, low temperature operation of CMOS circuits has been receiving substantial attention owing to advantages in speed performance, latchup immunity, and relaxed scaling restrictions[1]. On the other hand, BiCMOS circuits for driving large capacitive loads have been proved to be helpful in raising the speed performance[2]. However, BiCMOS circuits operating at $77K$ have received little attention due to degradation in the performance of bipolar devices at reduced temperatures[3]. In fact, operation of BiCMOS circuits at 77K can be justified if the performance of bipolar device can be improved for operation at $77K$. In order to investigate the feasibility of low temperature operation of BiCMOS circuits, a device-level study on the steady state and transient behavior of a $1\mu m$ BiCMOS inverter operating at $77K$ using a modified PISCES program with appropriate low temperature device models and a large-scale simulation capability is now described.

In the PISCES program[4], existing models of incomplete ionization, concentration and E-field dependent mobilities, and Auger recombination with concentration dependent lifetimes are not sufficient for low temperature simulation. In order to facilitate low temperature simulation of BiCMOS circuits, low temperature models in the PISCES program have been added. The appropriate models used in the low temperature simulation include Fermi-Dirac statistics, incomplete ionization, bandgap narrowing, concentration and E-field dependent mobilities, Shockley-Read-Hall and Auger recombinations with concentration dependent lifetimes[4]. In order to overcome the convergence difficulties for low temperature simulation, Newton's method with Gaussian elimination of the Jacobian for two-carrier simulations with a modified scaling is used[5]. Using the modified PISCES program, turn-on transient performance of BiNMOS and BiPMOS devices at 77K has been reported[6][7]. Here, low temperature performance of a BiCMOS inverter operating at 77K has been analyzed using the modified low temperature PISCES program with an upgraded large-scale simulation capability.

Fig. 1(a) shows the device cross section of a BiCMOS inverter based on a $1\mu m$ BiCMOS technology[8] used in studying the low temperature performance. The NMOS and PMOS devices have an effective channel length of $0.9\mu m$, and a gate oxide thickness of 250Å and threshold voltages of $0.8V$ and $-0.8V$, respectively. Fig. 1(b) shows the vertical doping profile in the intrinsic and the extrinsic base regions. The intrinsic base has a width of $0.1\mu m$ and a peak concentration of $1 \times 10^{18} cm^{-3}$. In order to meet the grid limit, NMOS, PMOS and bipolar devices are placed against one another separated by oxide layers. The bases of the two bipolar devices and the source/drain terminals are wired together with parasitic capacitances of $0.1fF$ and a capacitive load is $0.1pF$ at the output.

Figs. 2 and 3 show the steady state performance of the NMOS and PMOS devices used in the BiCMOS inverter. Fig. 2(a) shows the I_D vs. V_{GS} curves of the NMOS device for $V_{DS} = 0.1V$ and $3V$. The subthreshold slope improves about 3.8 times at $77K$. Due to the $0.9\mu m$ channel length, the drain induced barrier lowering effect is slightly less at $77K$. As shown in Fig. 2(b), in the saturation region, the drain current at $77K$ improves about 50% owing to enhancement in the electron mobility. As for the PMOS device, Fig. 3(a) shows the I_S vs. V_{GS} curves for $V_{DS} = -0.1V$ and $-3V$. As in experimental results, the delayed turn-off phenomenon at weak inversion[9] is observed as a result of the incomplete ionization in the buried channel. As shown in Fig. 3(b), in the saturation region, the improvement in the PMOS source current at $77K$ is over 50% owing to enhancement in the hole mobility. Fig. 4 shows the steady state performance of the bipolar device. At $77K$, the current gain as shown in Fig. 4(a) degrades 10× due to the bandgap narrowing effect. As shown in Fig. 4(b), at $77K$, at a current below $10^{-5} A/\mu m$, the base resistance is larger due to carrier freezeout effects and and is smaller at a current above $10^{-5} A/\mu m$ owing to a higher mobility. As shown in Fig. 4(c), at $77K$, the peak value in f_T is smaller due to the presence of compensating donor levels. As shown in Fig. 4(d), at $77K$, the zero-bias base-to-emitter capacitance is smaller due to a higher built-in voltage. On the other hand, the diffusion capacitance is much higher at a high current due to a lower thermal voltage at $77K$.

For a BiCMOS inverter, steady state performance of devices cannot describe the behavior of the circuit during transient. In order to study the overall performance of the BiCMOS inverter at 77K, transient analysis is now described. By imposing a voltage pulse between $0V$ and $5V$ with rise and fall times of $10ps$ on the input, pull-up and pull-down transient behavior of the BiCMOS inverter has been obtained at $300K$ and $77K$. Fig. 5 shows the base voltages of BiNMOS and BiPMOS devices during transient at $300K$ and $77K$. When the input turns high initially, there are overshoots in the base voltage of both BiPMOS and BiNMOS transistors around the edge of the input ramp owing to the displacement current effect. The $77K$ case shows higher overshoots in the base voltages of both bipolar transistors owing to a smaller base-to-emitter capacitance. After the ramp-up period, the BiNMOS transistor turns on with a steady base voltage and the BiPMOS base voltage slews in the negative direction. At $1ns$, the bipolar device of the BiPMOS transistor turns on and its base voltage may exceed 5V[9]. At $77K$, the internal voltage overshoot is much smaller owing to a much larger diffusion capacitance. As the emitter voltage approaches 5V, the base-to-emitter voltage is decreasing, indicating the removal of the carriers from the base area. Fig. 6 shows the output voltages at $300K$ and $77K$ during transient. The fall time, defined as the time from the middle of the input swing during the ramp-up period to the middle of the output swing, degrades from $0.375ns$ at $300K$ to $0.507ns$ at $77K$ due to a smaller collector current and a larger base diffusion capacitance in the BiNMOS transistor despite a smaller base resistance and a larger NMOS drain current at $77K$. On the other hand, the rise time, defined as time from the middle of the input swing during the ramp-down period to the middle of the the output swing, at $77K$ and $300K$ is about identical. This is attributed to a smaller output swing at $77K$ and a less non-negligible collector current in the BiNMOS transistor, as shown in Fig. 7, as a result of not fully turn-off of the bipolar device of the BiNMOS during the pull-up transient. Fig. 8 shows the electron concentration contours of the two bipolar devices of the BiNMOS and BiPMOS transistors as the BiPMOS emitter current reaches its peak in magnitude at $1300ps$. At $77K$, much fewer electrons exist in the bipolar area of the BiPMOS transistor as the BiPMOS device is fully turned on and much fewer electrons are present in the bipolar area of the BiNMOS device as the BiNMOS is turning off. Fig. 9 shows the total electrons minus initial total electrons ($Q_{nt} - Q_{ndc}$) in each bipolar area during transient. During pull-up transient, at $77K$, the difference in the ($Q_{nt} - Q_{ndc}$) in the bipolar area of the BiPMOS device between the $77K$ and $300K$ cases is smaller than that of the BiNMOS device during the pull-down transient. On the other hand, the speed of the electron removal in the BiNMOS device is quicker at $77K$ during the pull-up transient as compared to the pull-down. This is why, at $77K$, the switching speed is slower during the pull-down transient and about identical during the pull-up transient as compared to $300K$. In conclusion, circuit and device designs can be optimized to justify the operation of BiCMOS circuits at $77K$.

Acknowledgments

The authors would like to thank Prof. R. W. Dutton of Stanford University for helping us obtain the license to use the PISCES program. This work is supported under R.O.C. National Science Contracts #NSC79-0404-E0002-21.

References

[1] "Low Temperature Electronics,", IEEE Press Book, 1986
[2] G. P. Rosseel and R. W. Dutton, "Influence of Device Parameters on the Switching Speed of BiCMOS Buffers," IEEE J. of Solid-State Cir. 2/89
[3] J. D. Cressler, D. D. Tang, K. A. Jenkins, G. P. Li, and E. S. Yang, "On the low-temperature static and dynamic properties of high-performance silicon bipolar Transistors," IEEE Tran. ED, 8/89
[4]M. R. Pinto, C. S. Rafferty, R. W. Dutton, "PISCES-2B: Poisson and Continuity Equation Solver," Technical Report, Stanford Univ., 9/84
[5] Y. W. Chen, K. H. Lou and J. B. Kuo, "Two-Dimensional Analysis of a BiNMOS Transistor Operating at $77K$," to be published on IEEE Tran. ED
[6] Y. W. Chen, K. H. Lou and J. B Kuo, "Two-Dimensional Transient Analysis of a BiNMOS Transistor Operating at $77K$ Using a Modified PISCES Program, Proc. of IEEE VLSI Process/Device Modeling Workshop, 8/90
[7] Y. W. Chen, K. H. Lou and J. B. Kuo, "Two-Dimensional Transient Analysis of a BiPMOS Transistor Operating at $77K$ Using a Modified PISCES Program, IEEE International Electron Devices Material Symposium, 11/90
[8] H. Iwai, et. al., "$0.8\mu m$ BiCMOS Technology with High f_T Ion-Implanted Emitter Bipolar Transistor," IEEE Digest of IEDM,1987
[9]F H. Gaensslen and R. C. Jaeger, "Temperature Dependent Threshold Behavior of Depletion Mode MOSFETs," Solid State electronics, 1979

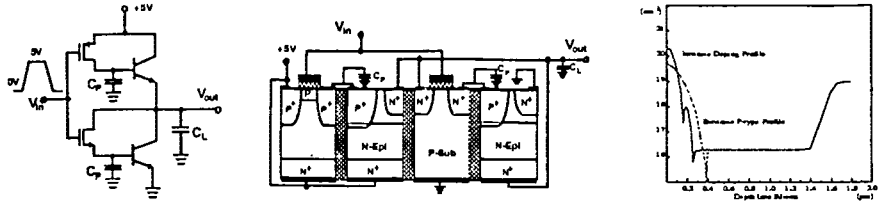

Fig. 1 (a) The BiCMOS device structure under study. (b) Vertical doping profiles in the intrinsic and the extrinsic base areas.

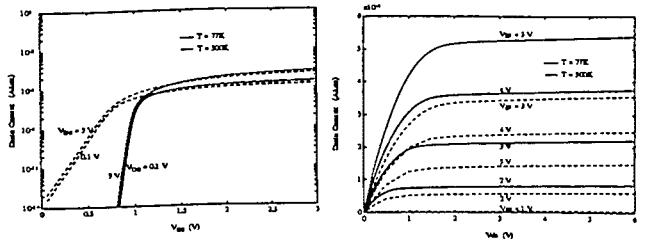

Fig. 2 (a) The I_D vs. V_{GS} curves of the NMOS device, used in the BiCMOS transistor, biased at V_{DS} of $0.1V$ and $3V$ for the $77K$ and $300K$ operations. (b) The I_D vs. V_{DS} curves of the NMOS device biased at V_{GS} from $1V$ to $5V$ for the $77K$ and $300K$ operations.

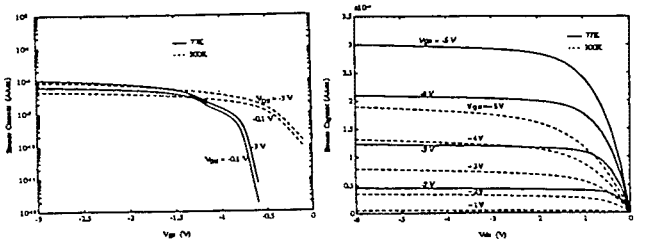

Fig. 3 (a) The I_S vs. V_{GS} curves of the PMOS device, used in the BiCMOS transistor, biased at V_{DS} of $-0.1V$ and $-3V$ for the $77K$ and $300K$ operations. (b) The I_S vs. V_{DS} curves of the PMOS device biased at V_{GS} from $-1V$ to $-5V$ for the $77K$ and $300K$ operations.

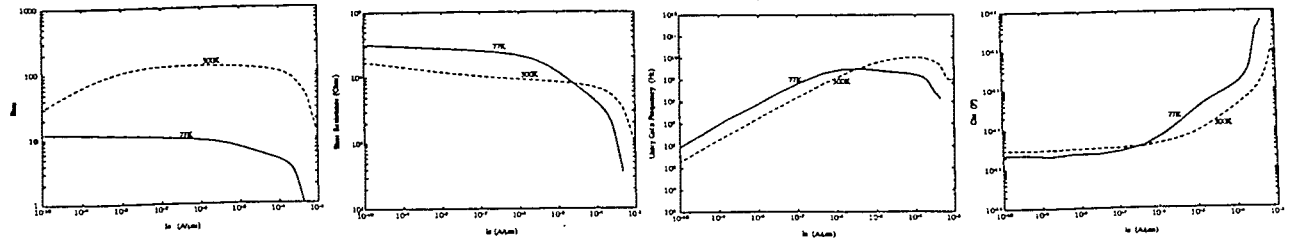

Fig. 4 Small signal steady state performance of the bipolar device used in the BiCMOS transistor, biased at a V_{CE} of $3V$ for the $77K$ and $300K$ operations. (a) The current gain. (b) The base resistance. (c) The unity gain frequency. (d)The equivalent base-to-emitter capacitance.

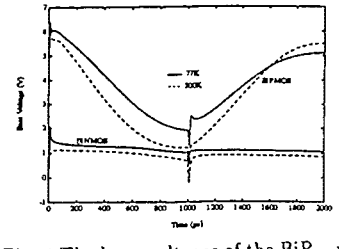

Fig. 5 The base voltages of the BiPMOS and BiNMOS devices during the transient for both $300K$ and $77K$ operations.

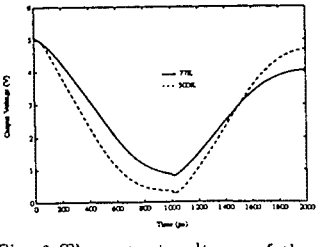

Fig. 6 The output voltages of the BiCMOS with output load of $0.1pf$ during the transient for both the $300K$ and $77K$ operations.

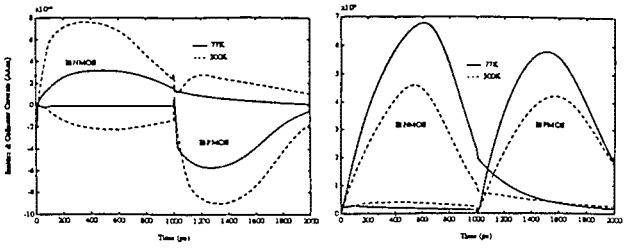

Fig. 7 The emitter currents of the BiPMOS device and the collector currents of the BiNMOS device for both $300K$ and $77K$ during the transient.

Fig. 9 Total electrons minus initia total electrons ($Q_{nt} - Q_{ndc}$) in th two bipolar transistors during tran

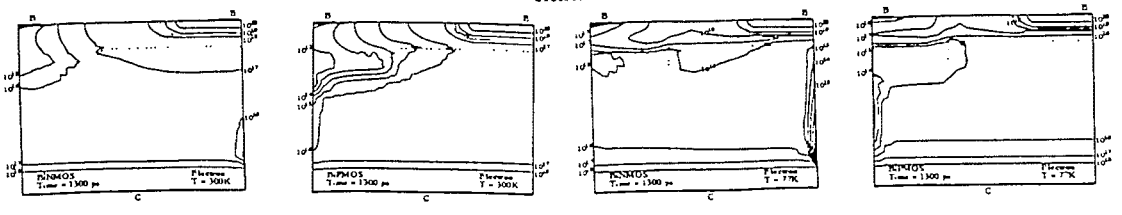

Fig. 8 Electron concentration contours in the two bipolar devices of the BiNMOS and BiPMOS transistors at $1300ps$ for the $300K$ and $77K$ cases.