LOW SUPPLY VOLTAGE BiNMOS OPERATION ANALYSIS USING A FULL DEVICE SIMULATION ON A BiNMOS GATE CIRCUIT

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Purposes Low supply voltage BiCMOS operation[1] has been a crucial issue and analysis[2] based on conventional circuit simulation has been reported so far. The performance of a *full* BiNMOS gate circuit, using a two-dimensional device simulator (MOS2C[3]), has been analyzed for the first time. (Up to now, a simulation[4] combining one bipolar and one MOSFET has been the newest report.) This paper clarifies the mechanism of propagation delay time increase for reduced supply voltage V_{CC}, based on carrier movements in individual devices during BiNMOS circuit operation.

Simulation method and results

Four devices (npn-bipolar, PMOSFET, 2 NMOSFETs) composing a BiNMOS gate circuit (Fig. 1(a), (b)) were simulated at the same time including two connection wires, as shown in Fig. 1(c), (d). A stable solution with sufficient accuracy was obtained by optimizing the matrix solver.

The transient response for a BiNMOS gate circuit (Fig. 2) and terminal current performance (Fig. 3) were simulated. Figure 1 shows typical hole current-vector distributions (c) for the rise and (d) fall times. In fall time discharging the base charge, the hole current direction is opposite to that for rise time and voltage between base and emitter is still maintained (Fig. 2). Therefore current flows through V_{CC} terminal to ground as shown in Fig. 3, resulting power consumption and other problems.

Experimental results and discussion for reduced supply voltage

A solid line in Fig. 4 shows the experimental result for measuring the BiNMOS propagation delay time, as a function of supply voltage. The delay times derived from the corresponding simulated transient response (Fig. 2) are shown with a dashed line. The simulated result agreed with the experimentally observed result with a more than two times increase in the delay time for V_{CC}=2V, as against 3V.

The rising time contribution to the delay time is larger in a basic BiNMOS gate circuit, as shown in Fig. 2 and Table 1. The rising time is divided into the base charging period t_B and the period for load capacitance charging by the bipolar t_C, as is broken down in Table 1.

Figure 3 compares the transient V_{CC} terminal current and the base current for V_{CC}=3 V and 2 V. In the rising period, the first V_{CC} terminal current peak corresponds to *on* for the PMOSFET and the second peak, after activating the bipolar, corresponds to the rising of the collector current I_C. With the reduction in V_{CC} from 3V to 2V, the delay for I_C to reach the peak value becomes marked. Consequently, the rising slope for the output voltage becomes smaller than that for the base voltage for V_{CC}=2V in Fig. 2. This effect is attributed to the main part of the increase in the propagation delay time.

Conclusion A new device simulation method has been developed, which can be used to analyze the circuit performance for various kinds of BiNMOS gate in a real circuit environment, and based on the carrier movement in each device. This method provides more useful information than that expected by conventional circuit simulation, to design miniaturized BiCMOS devices.

References 1)H.Momose, et al., IEDM Tech. Dig., 838('87) and 231('90) 2)A.Watanabe, et al., IEDM Tech. Dig., 429('89) 3)T.Kobori, NUPAD III, 75('90) 4)J.Kuo, et al., ED-37, 1308('90)

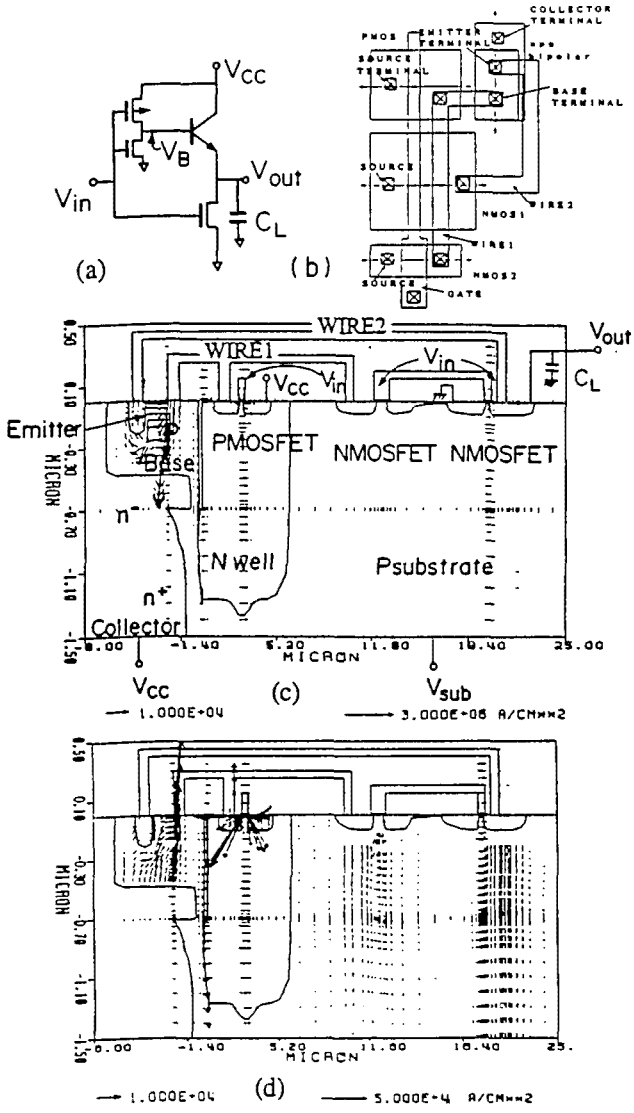

Fig. 1 (a), (b) Simulated BiNMOS gate circuit and (c) simulated region including 4 devices. Simulated hole current-vector distributions (c) at 3.6 ns (rise period) and (d) at 4.8 ns (fall period).

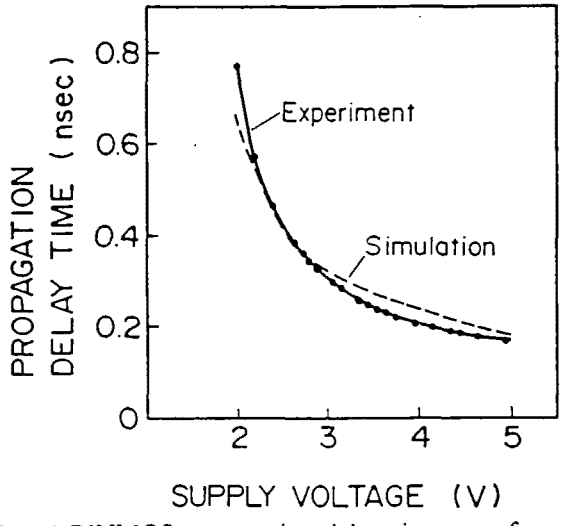

Fig. 4 BiNMOS propagation delay time as a function of supply voltage. Experimental results measured for fan-out 1, 41 stage ring oscillator. Simulated delay time derived from transient response.

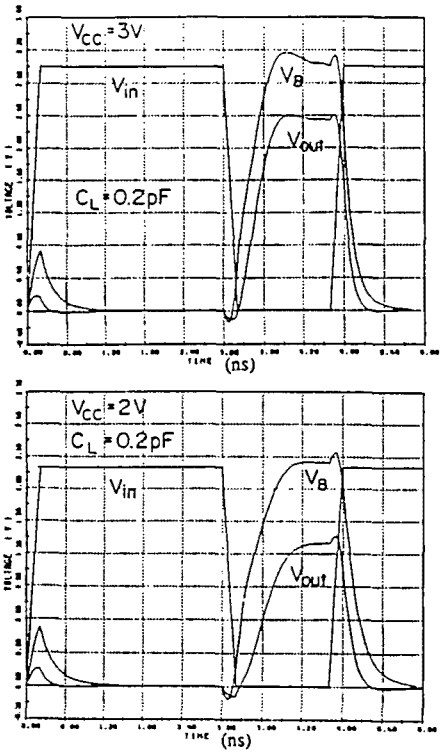

Fig. 2 Transient response of BiNMOS gate for V_{CC}=3 and 2 V. Before V_{in} is biased on and off, V_{in} and V_{CC} are pulled up at the same time for the first 200 ps and V_{in} is kept for a sufficient time to discharge the carrier.

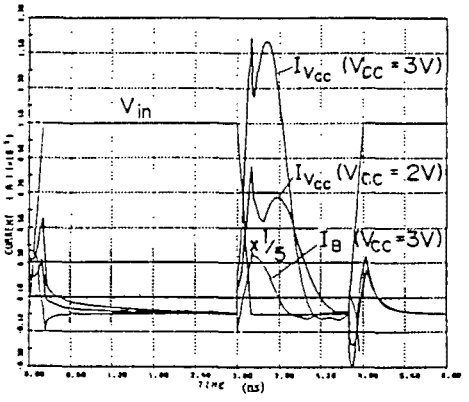

Fig. 3 Transient V_{CC} terminal current and base current I_B for V_{CC}=3, 2 V

	BiNMOS			CMOS	
(ns)	t_B	t_C	t_f	t_r	t_f
V_{CC}	t_r				
	τ_{pd} (=1/2(t_r+t_f))			τ_{pd}	
3V	0.22	0.25		0.62	0.26
	0.47		0.17		
	0.32			0.44	
2V	0.4	0.5		0.9	0.54
	0.9		0.4		
	0.65			0.72	

Table 1 Simulated delay times and their components of BiNMOS gate and CMOS inverter used in this BiNMOS gate.